TLP – Transient Liquid-Phase Bonding und andere neue Verfahren

Eltroplan Technologie-Tag
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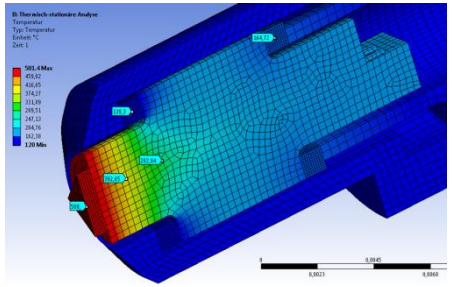
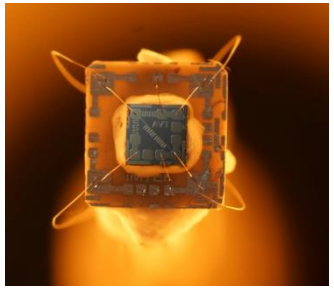
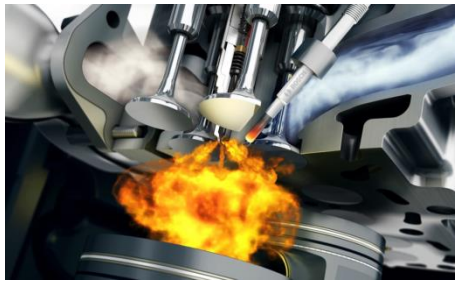
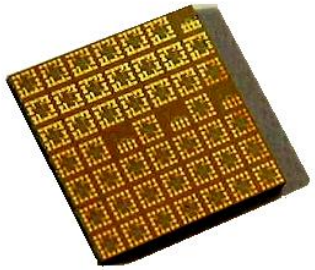
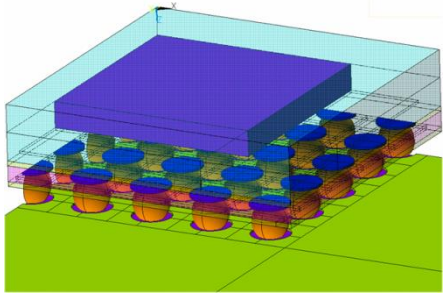
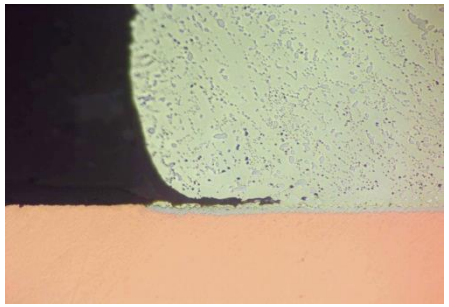
Schwerpunkte





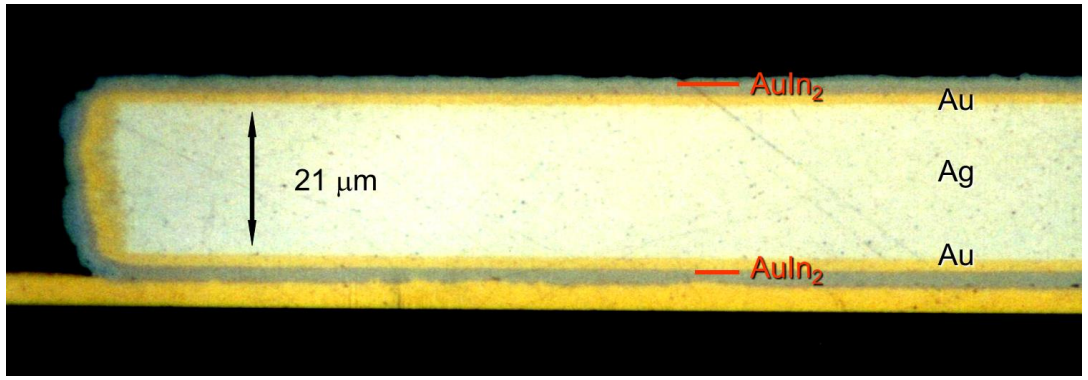
- Design-for-reliability auf Basis der Fehlerphysik
- Funktionale Optimierung von MEMS und Sensoren
- Lebensdauerprognose mechatronischer Systeme
- Techniken für Condition Monitoring und strukturintegrierte Sensoren
- Hochtemperatur-AVT für Sensoren bis 1000 °C

Alternative Die-Bonding Processes

Die-attach method	Material / Manufacturer	Bonding temperature	T_{max}
Electrically conductive adhesive	Silver filled epoxy Heraeus PC3001	120 – 180 °C	220 °C
Silver sintering	Silver paste Heraeus LPS 275	240 °C	961 °C
Transient liquid phase bonding	Multilayer foil Sn-Ag-Sn (IMTEK)	210 - 235 °C	650 °C
Klett-Welding	Cu-foil with nanowire brushes on both sides	180 - 235 °C	1.085 °C

Zuverlässige AVT für Mikrosysteme mittels TLP



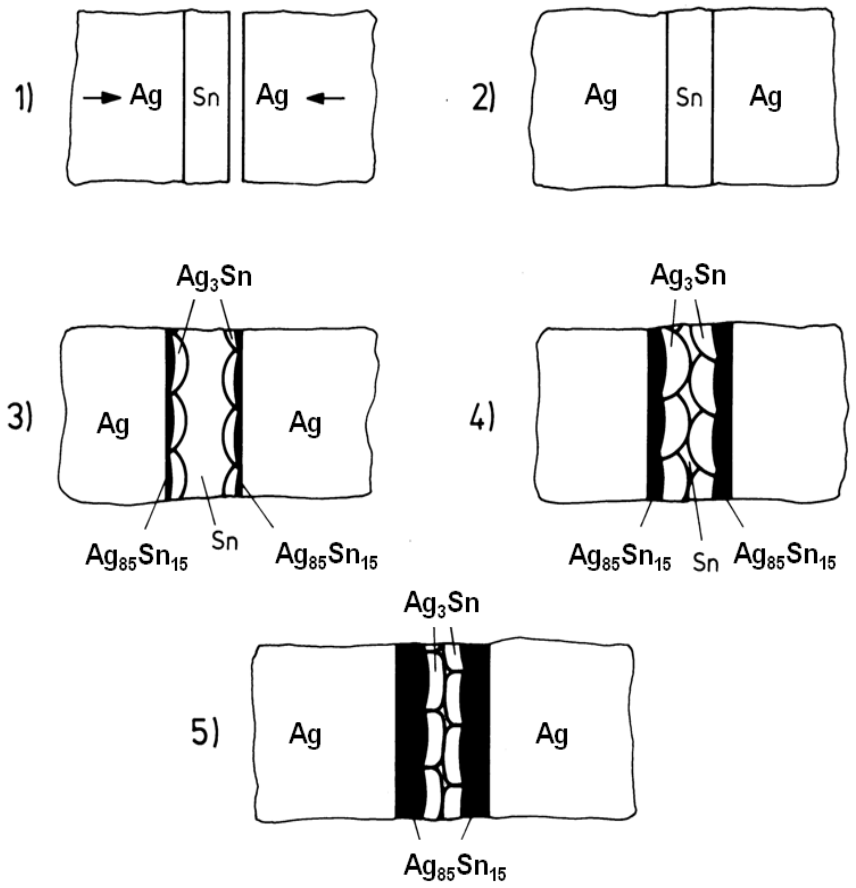
Solargeneratoren für Weltraumanwendungen Trends (1992)

- Zunehmender Einsatz fragiler GaAs-Solarzellen
- Dünnere Si-Zellen
- Größere Bruchempfindlichkeit bei Si und GaAs

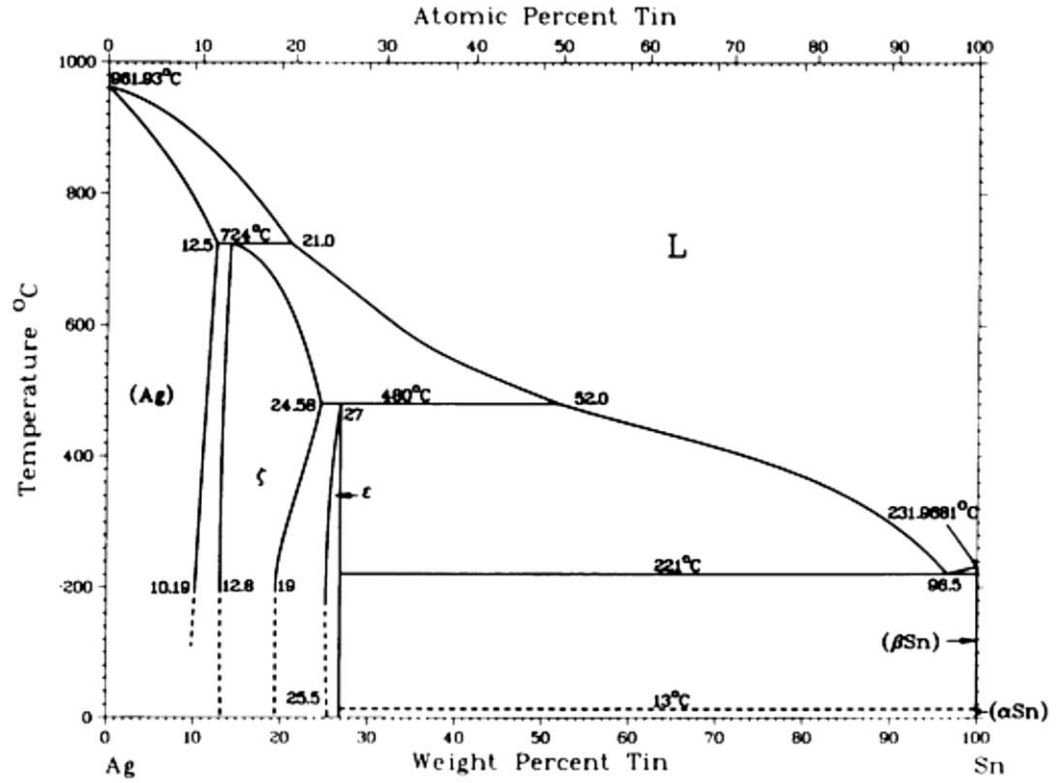
Ergebnis der Untersuchungen

- Entwicklung eines neuen, belastungsarmen Fügeverfahrens für Solarzellen mit Fügetemperaturen von $T < 300$ °C, z. B. mittels Isothermer Erstarrung (IE=TLP)

Transient Liquid-Phase Bonding (TLP) mit Ag-Sn-Phasen

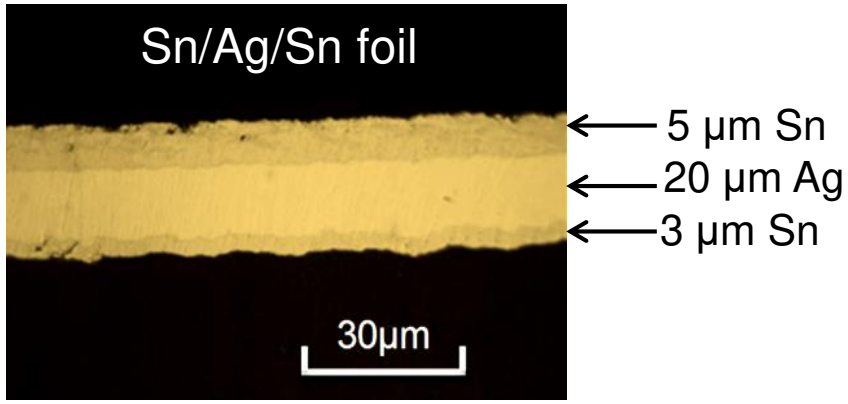


Transient Liquid-Phase Bonding (TLP, SLID)



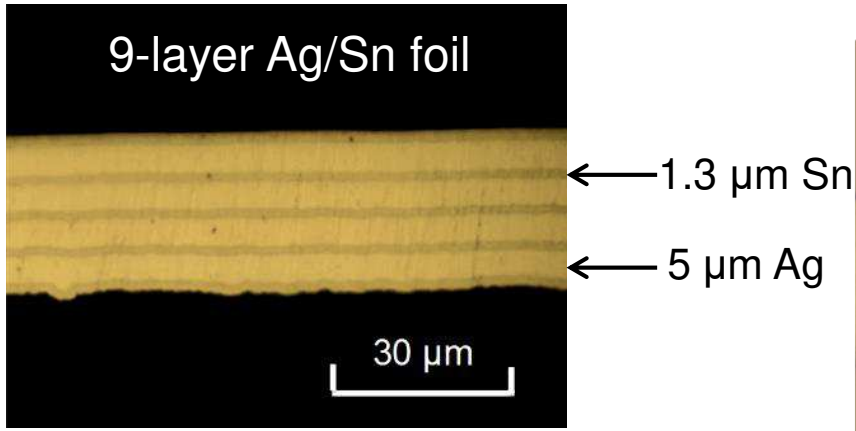
Binary system	Phase	Zusammensetzung m-% Sn	T_{Melt}
Ag-Sn	Ag	0 - 12.5	961 °C
	ζ (~$Ag_{85}Sn_{15}$)	12.8 - 24.6	> 650 °C
	ε (Ag_3Sn)	25	480 °C

Development of Multilayer-Systems – Electroplated Foils

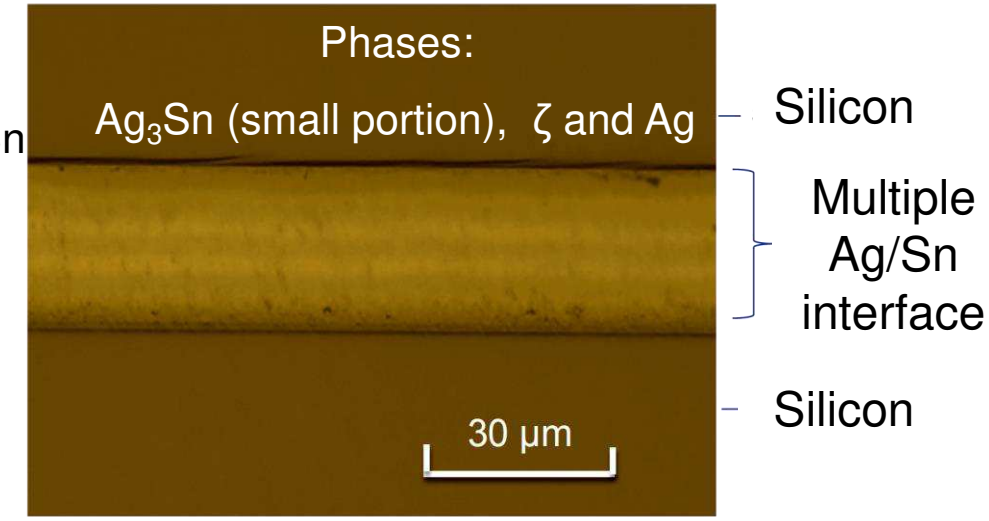


Advantages of multilayers

- Smaller diffusion length & shorter diffusion time
- Thicker bonding layers >30 µm
- More homogeneous composition
- Annealing after bonding can be avoided

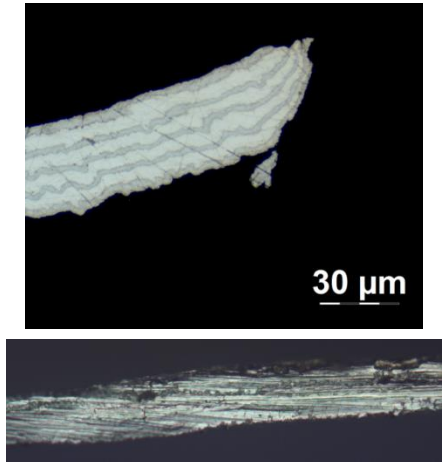


Cross sections of Sn-Ag based multilayered foils

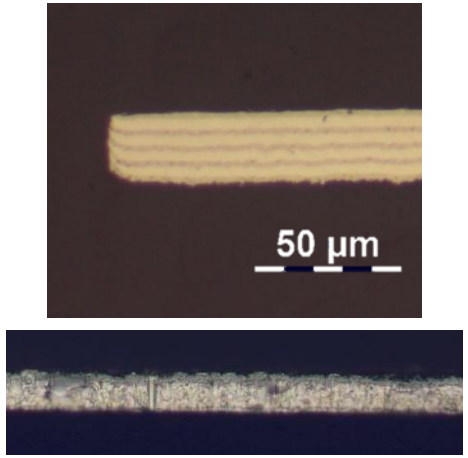


Vereinzeln der Folien – TLP-Preforms

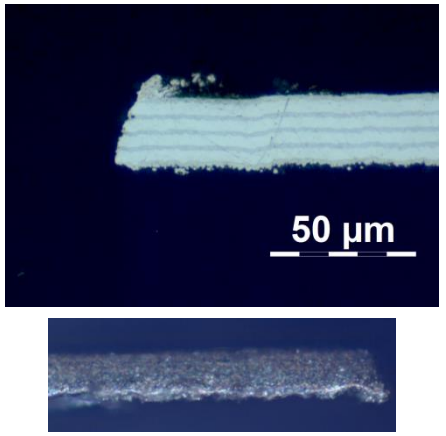
Skalpell



Stanzen (Fa. Pfarr)

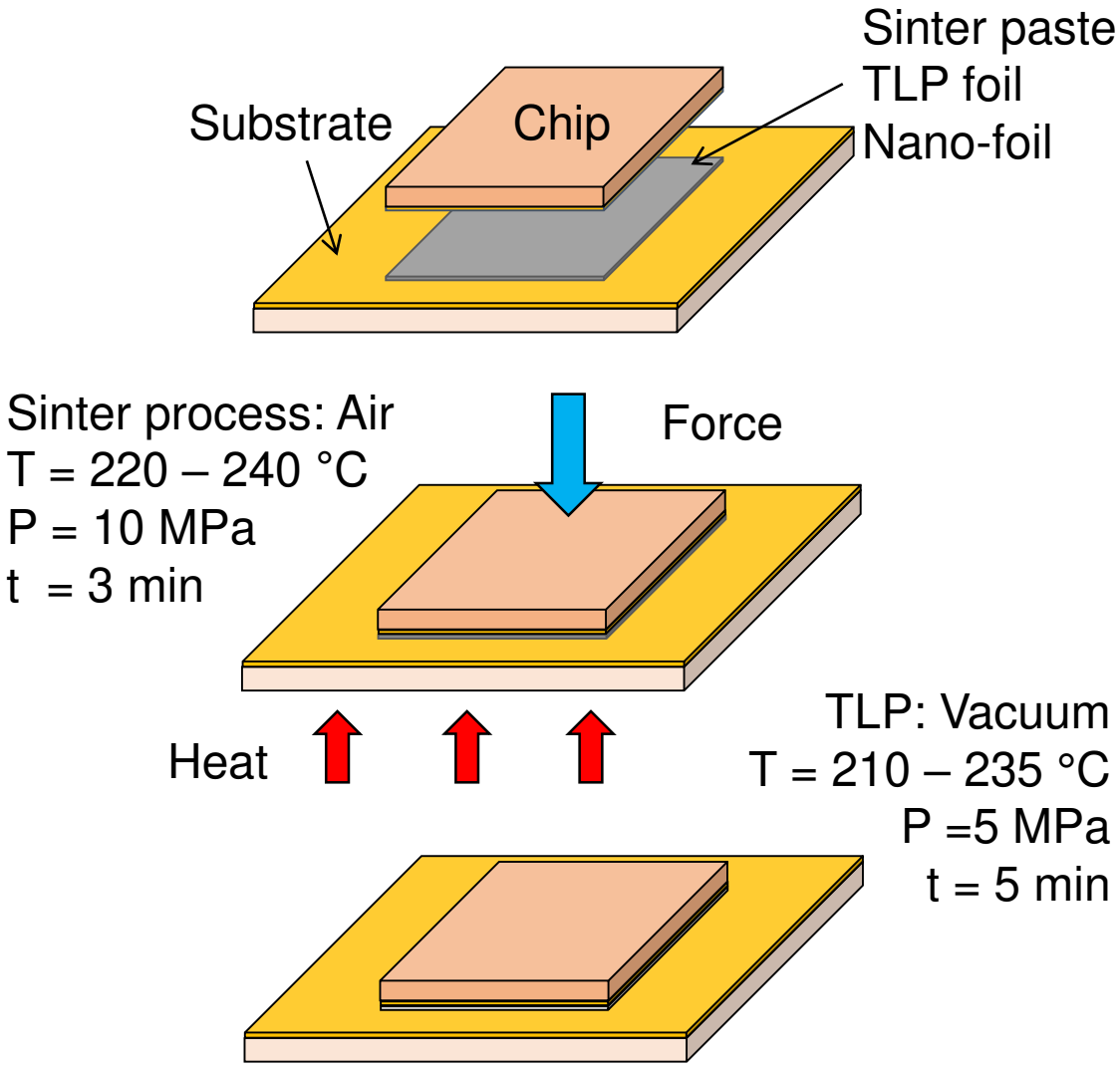


Laserschneiden



- **Schneiden**
  - Starke Deformation/Quetschung
  - Gratbildung
  - Hoher Aufwand
  - Nur für Labormaßstab nutzbar
  - Flexibel
- **Stanzen**
  - Saubere gerade Kanten
  - Keine Gratbildung
- **Laserschneiden**
  - Aufschmelzen und Reaktion
  - Optimierung nötig

Die Attachment Processes Sintering, TLP, KlettWelding



Dispensing /
Screen printing
Pick & place

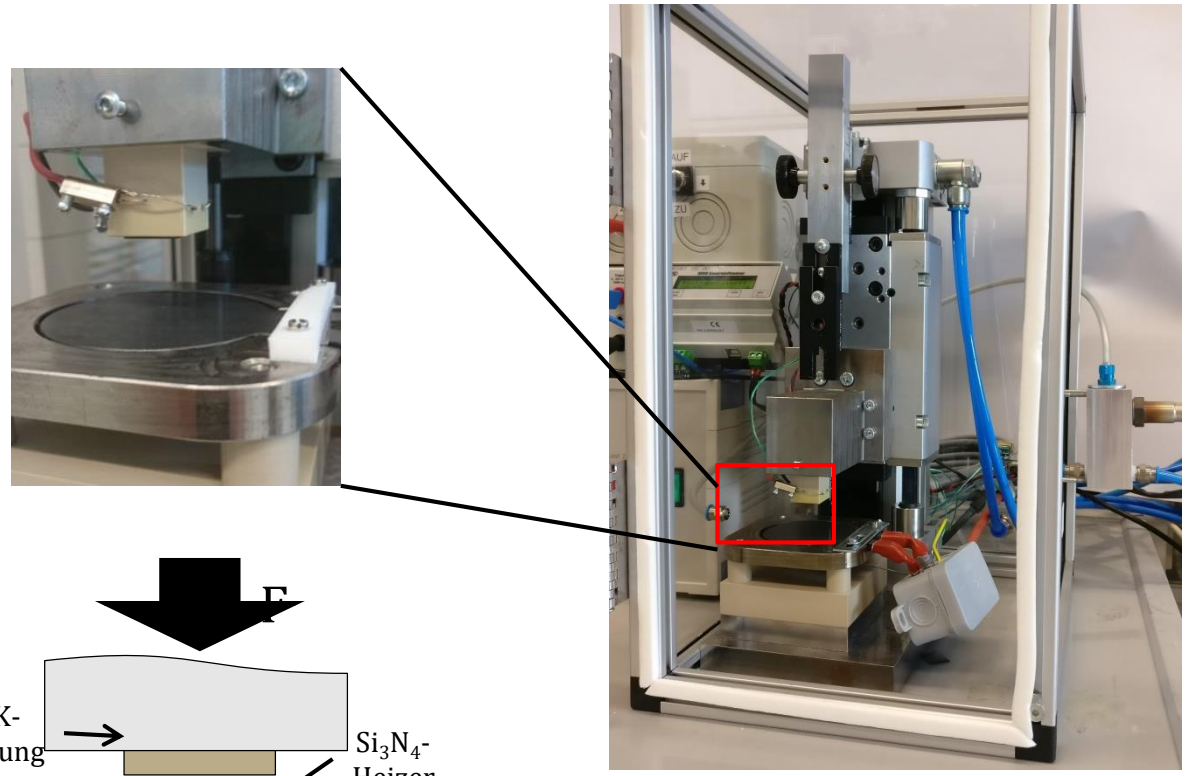
Pick & place
device

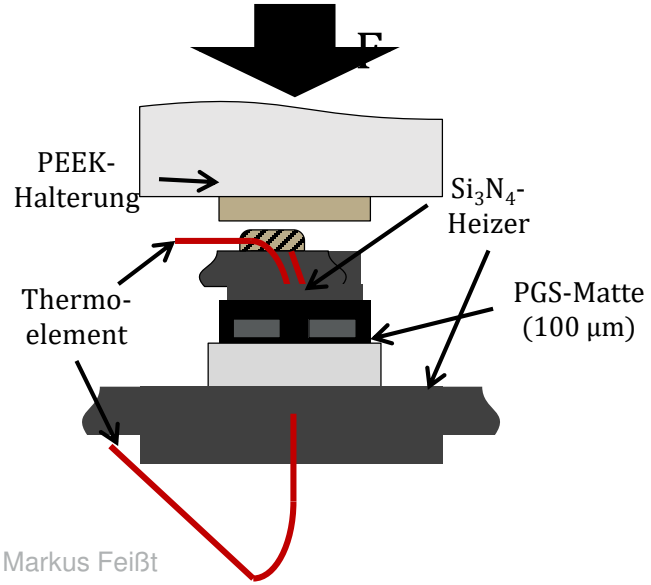
Sintering / TLP:
Pressure + temperature

Bondanlage für Einzelteile

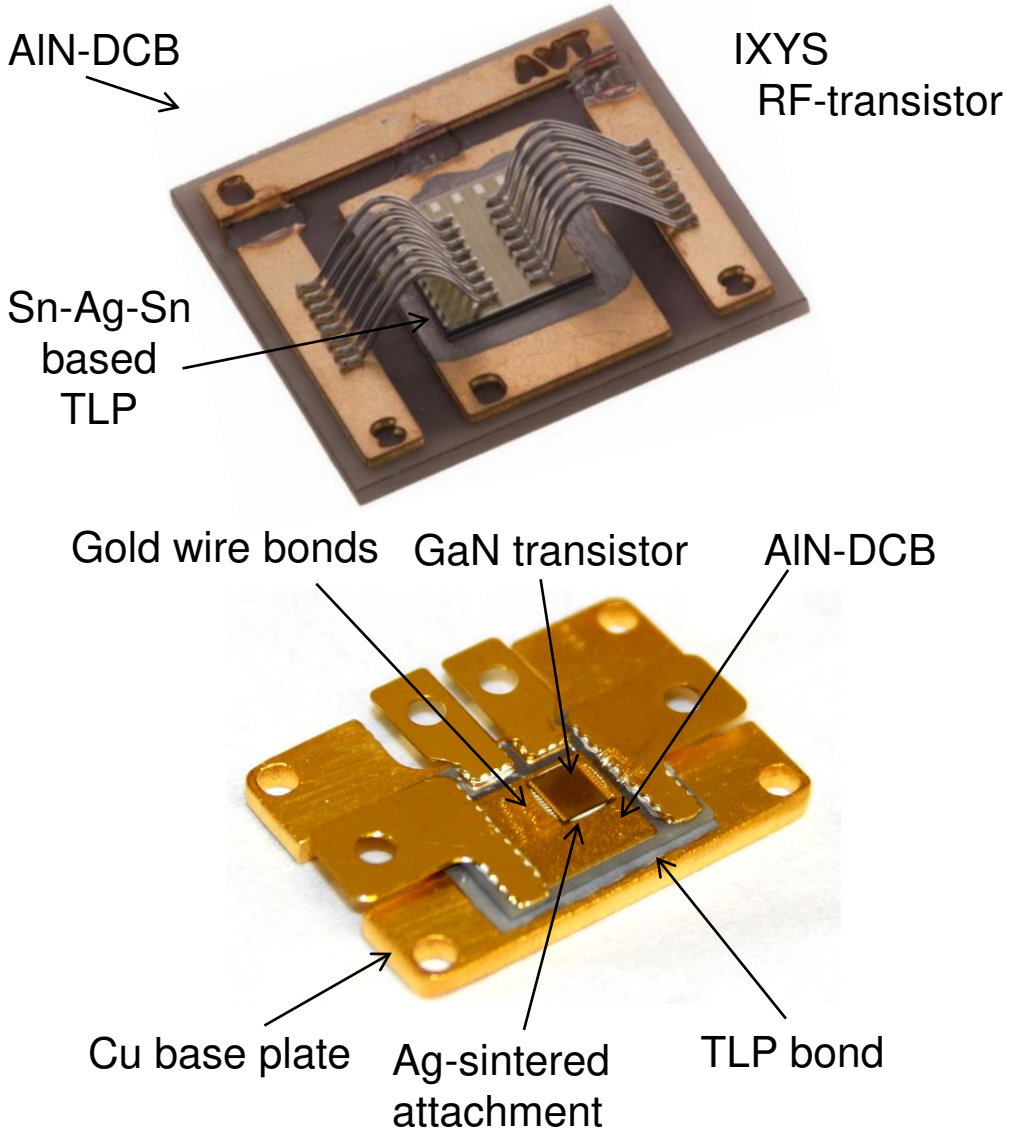
- Zielsetzung: Kurze Aufheizzeiten
- Aufbau:
  - Thermisch isolierte Si_3N_4-Heizer
  - Pneumatischer Linearantrieb
  - Atmosphäre: N_2
  - O_2-Sensor (Fa. Seho)
- Ermöglicht Analyse der Prozessparameter

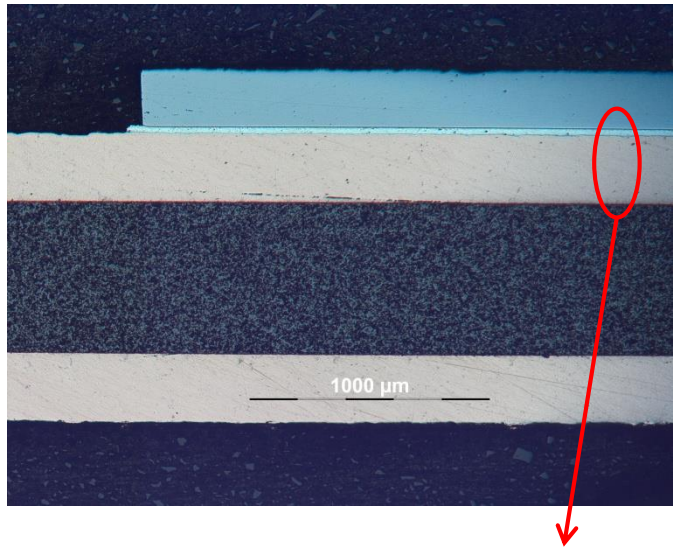
Spezifikation	
Heizraten	3,4 bis 25 K/s
Kraftbereich F	7,5 bis 700 N
Unsicherheit ΔF	~ 5 N
Restsauerstoffgehalt	~ 50 ppm

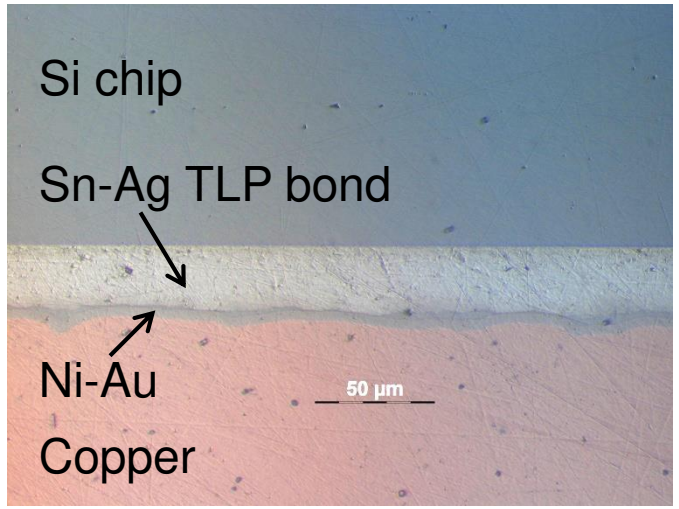




Assembled Devices After TLP-Bonding



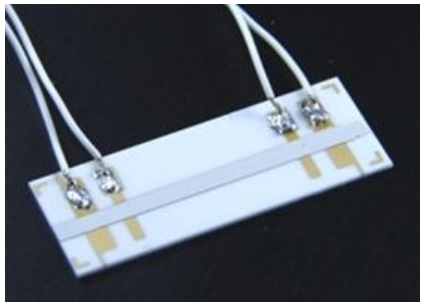




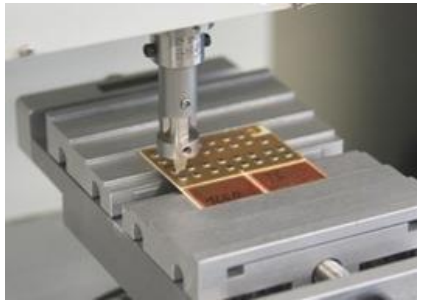
Analysen in Assembly & Packaging

Untersuchungen

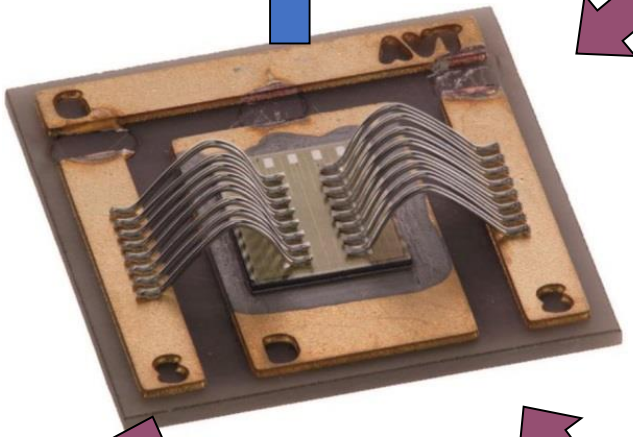
Drahtbonds **Die-Bonds**

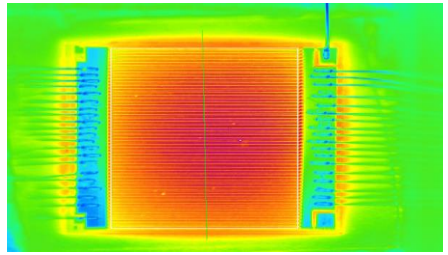


Elektrische Eigenschaften

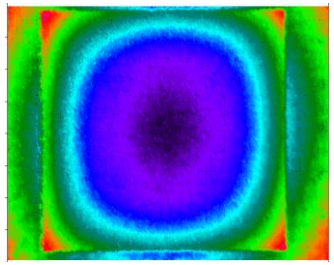


Scherfestigkeit



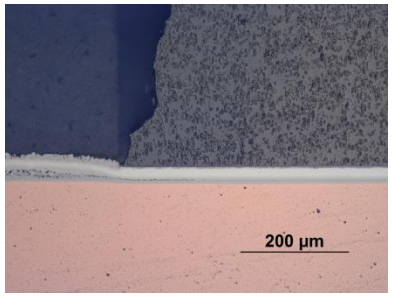


Thermischer Widerstand



"Stress"

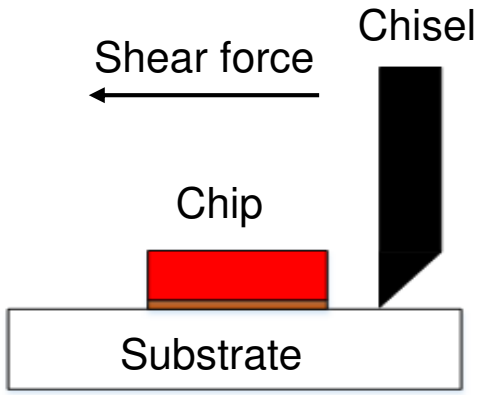
Zuverlässigkeit

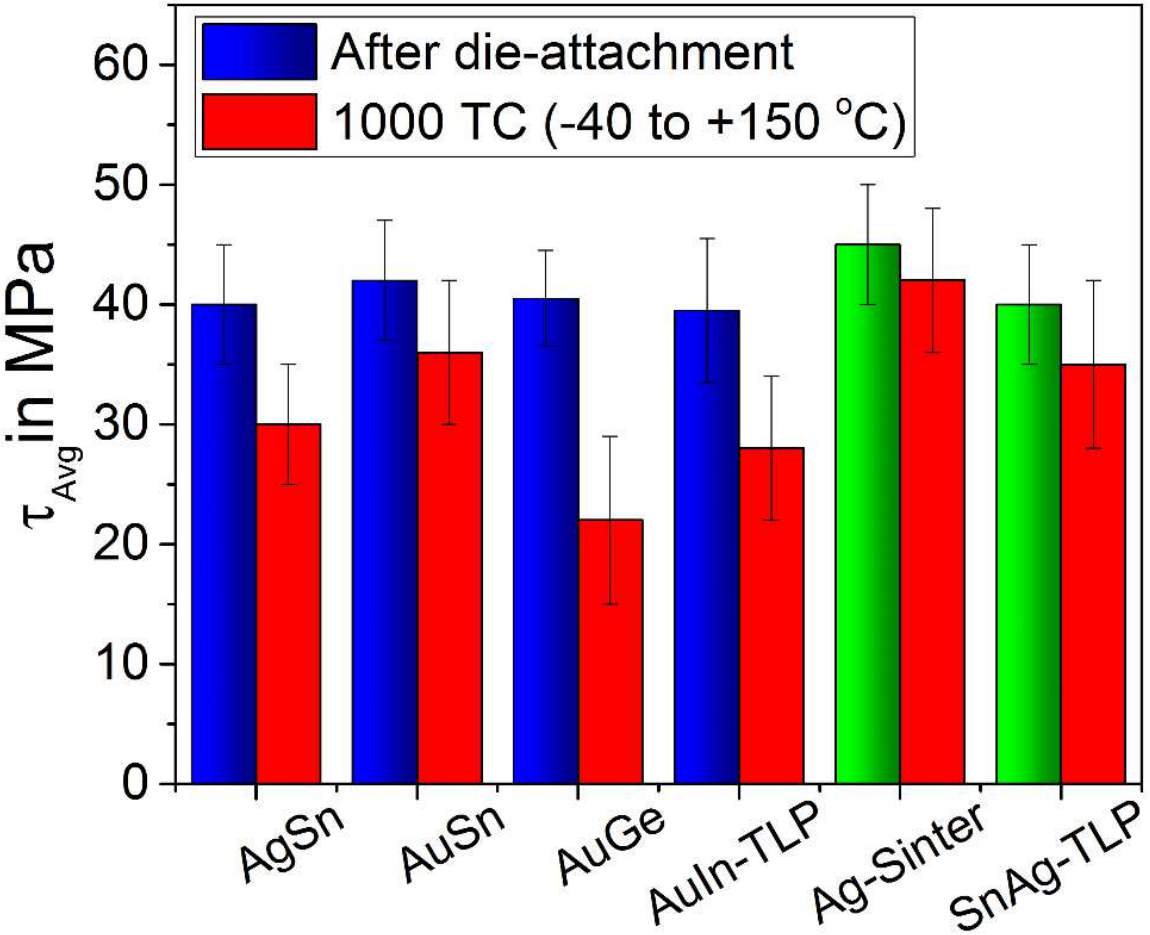


Fehleranalyse

Strength of Ag-Sintered and TLP-Bonded Joints on SiC-Diodes

- Passive temperature cycling from -40 to 150 °C
- Chips: SiC - diodes
- Sample size: 30
- Substrate: AlN DCB
- High die-shear strength

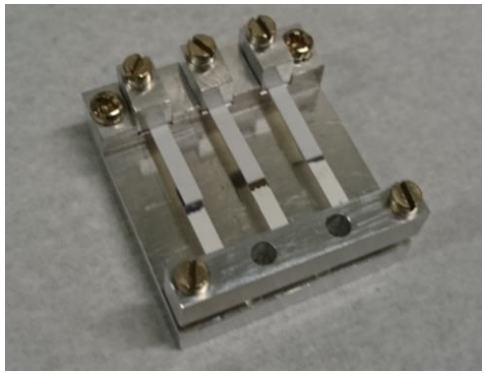




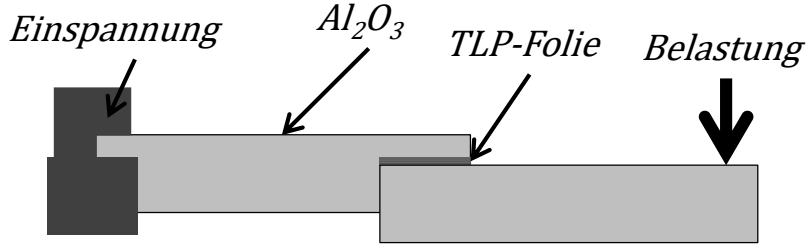
Sources: Own results (green-red)
Kim et al. 2009, Hagler et al. 2011, Wu et al. 2014)

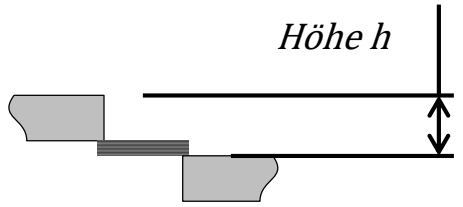
Prüfung der Temperaturstabilität

- Verbinden von Al_2O_3-Streifen
  - 10 min Bondzeit
  - Auslagern bei 200 °C für 12 h
- Einseitige Belastung (je drei Proben)
  - Heizen auf 300 °C, 350 °C bzw. 400 °C
- Analyse des Höhenunterschieds
  - Optischer Abstandssensor



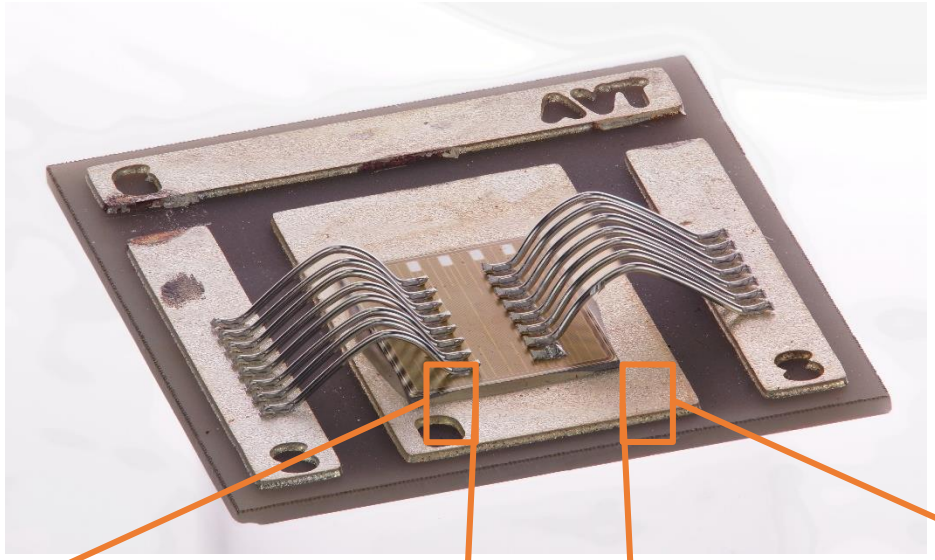
Ohne Auslagern	Nach Auslagern		
300 °C	300 °C	350 °C	400 °C
X	O	O	O
(X)	O	O	(X)
X	O	O	O



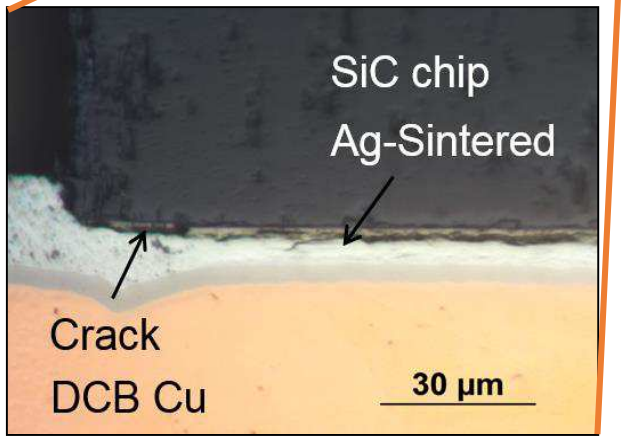


Keine Änderung O
Abstandsänderung (X)
Kein Kontakt X

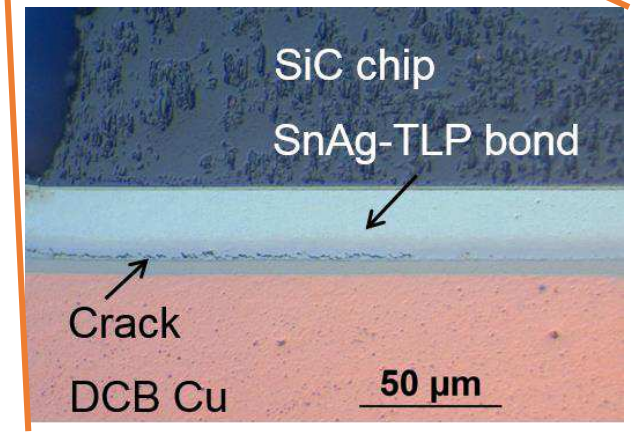
Reliability Assessment - Power Cycling



Sintered joint



Sintered bond

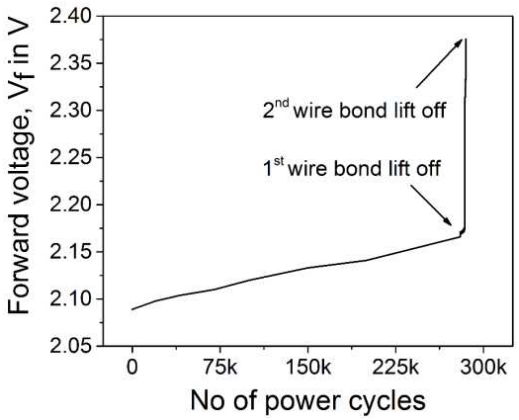


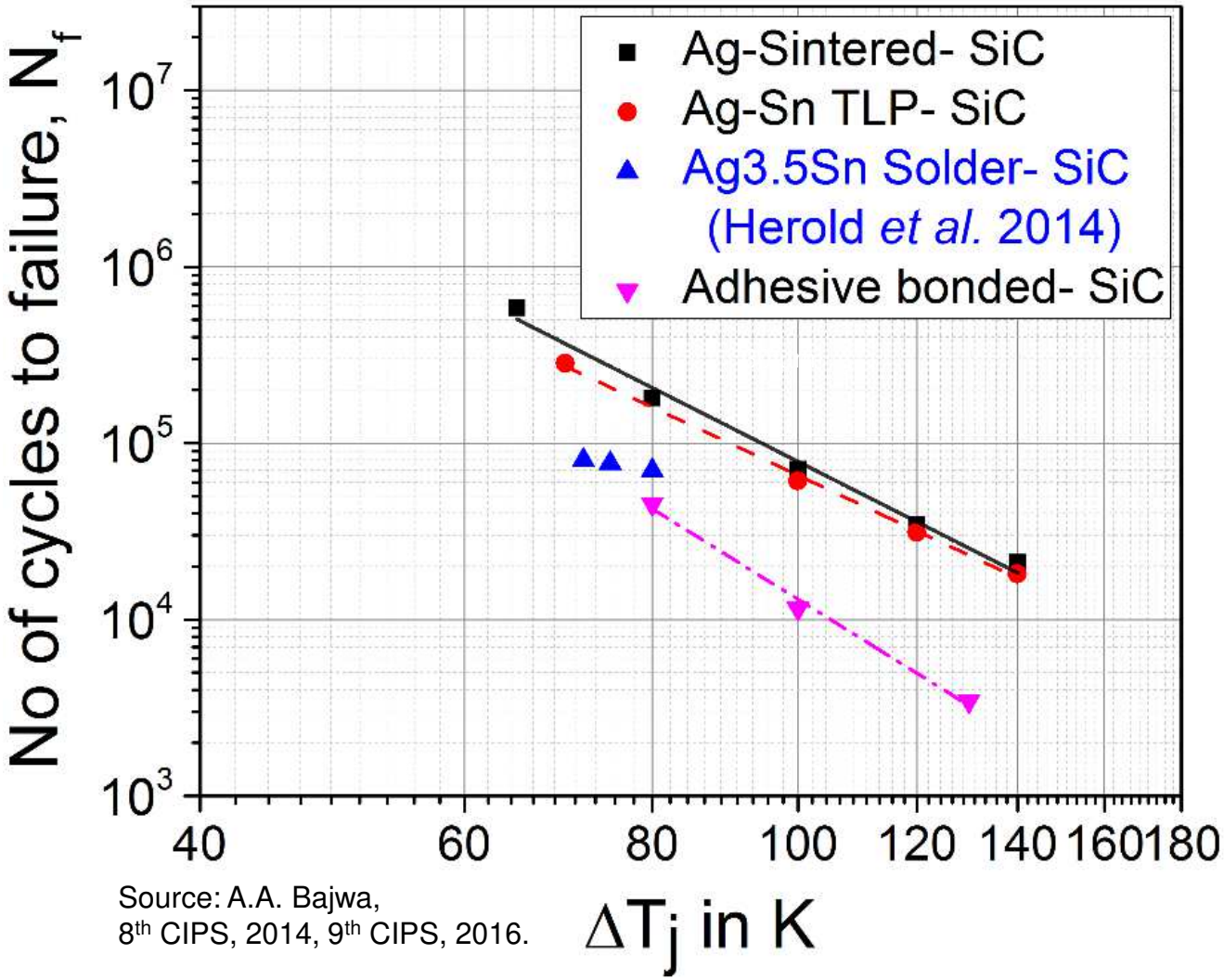
APC-Prüfstand

Power Cycling Life-time of SiC-Diodes on AIN-DCB

Power on-off-test

- I_f: 15 to 20 A
- V_f: 1.8 to 2.8 V
- t_{on}: 3 s,
- t_{off} = 3.5 s
- ΔT_j: 70 K to 140 K
- Failure criterion: +10 % of V_f





Source: A.A. Bajwa,
8th CIPS, 2014, 9th CIPS, 2016.

Bending Stresses in Assembly

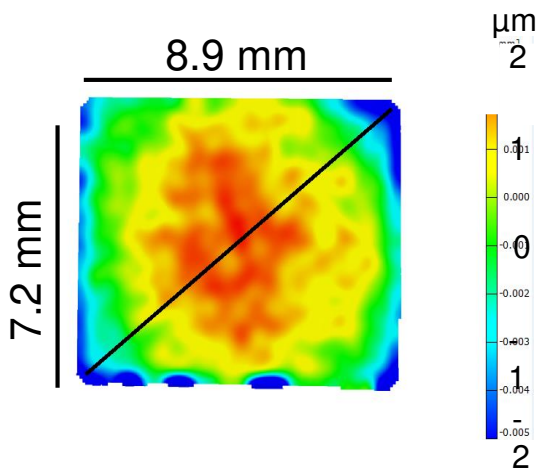
Warping in

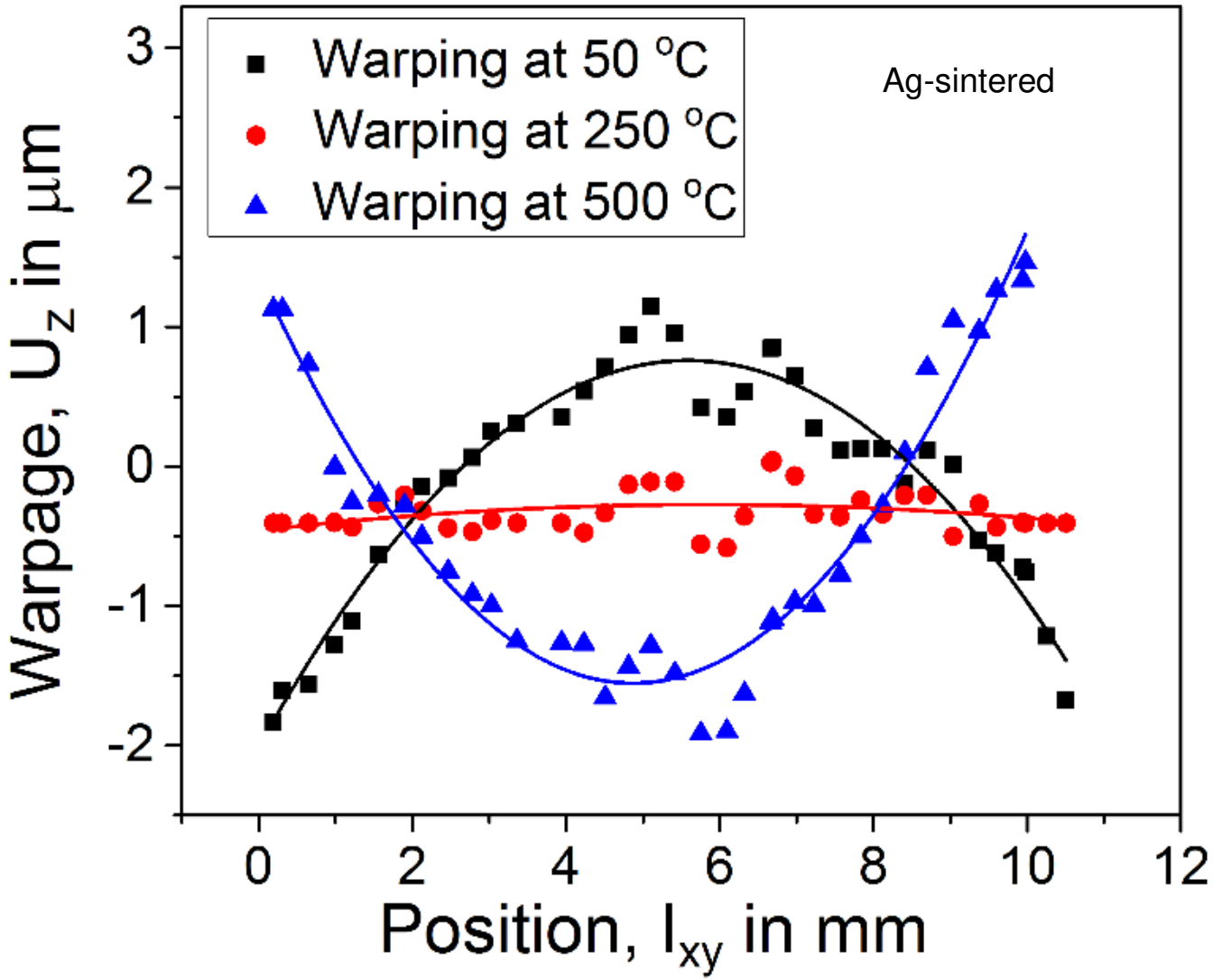
- Ag sintered
- Si chip
- on AlN DCB

  @ 50 °C

  @ 250 °C

  @ 500 °C

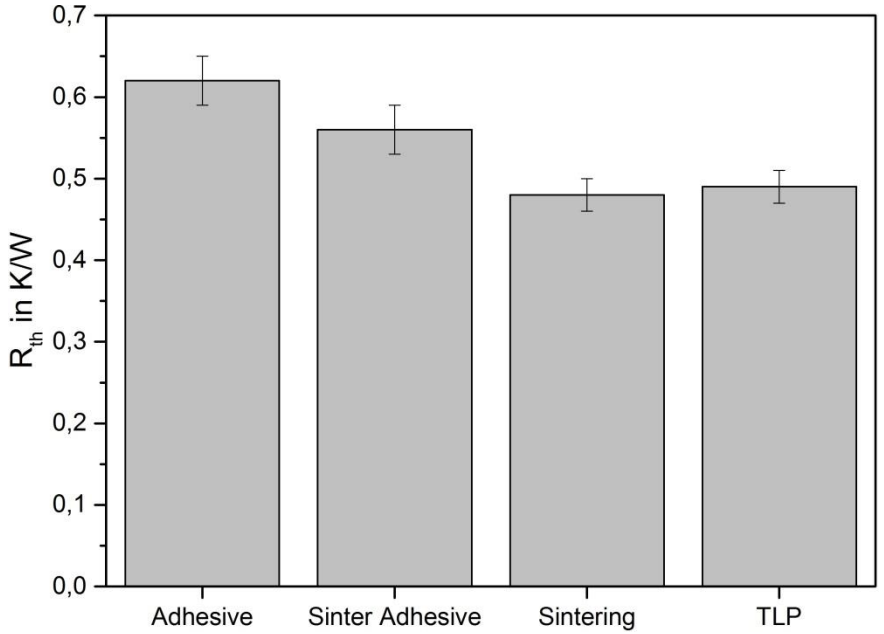




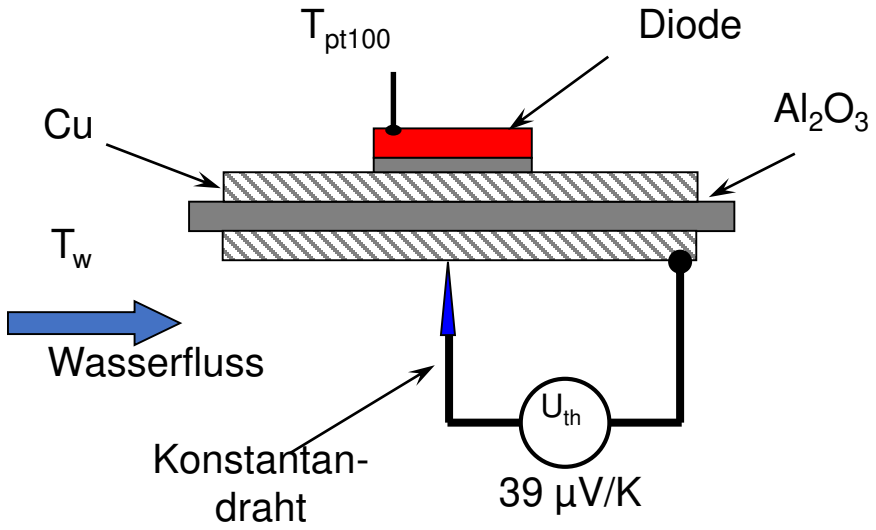
Charakterisierungsmethoden

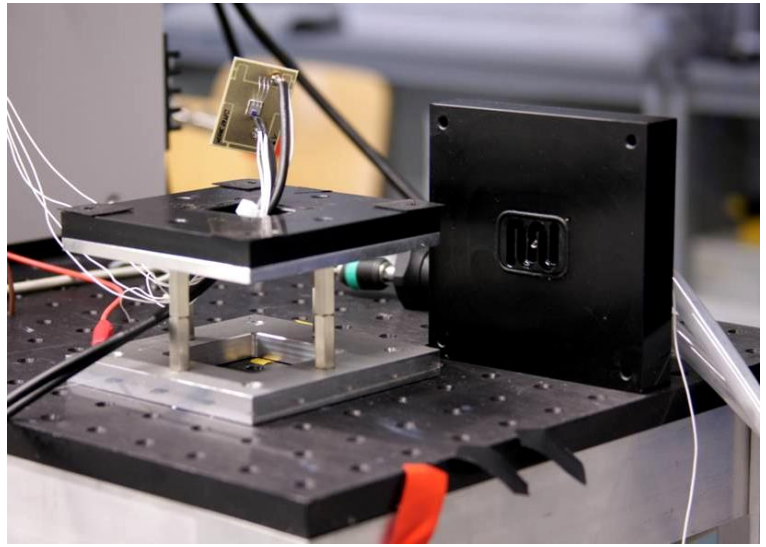
Elektrische und thermische Eigenschaften

- Thermischer Widerstand $R_{th} = \frac{\Delta T}{P}$ $R_{th} = d/\lambda \cdot A$



Mittelwert aus Stromwerten I = 2 – 18 A;
Diode 4,5 x 4,5 mm² auf DCB-Substrat

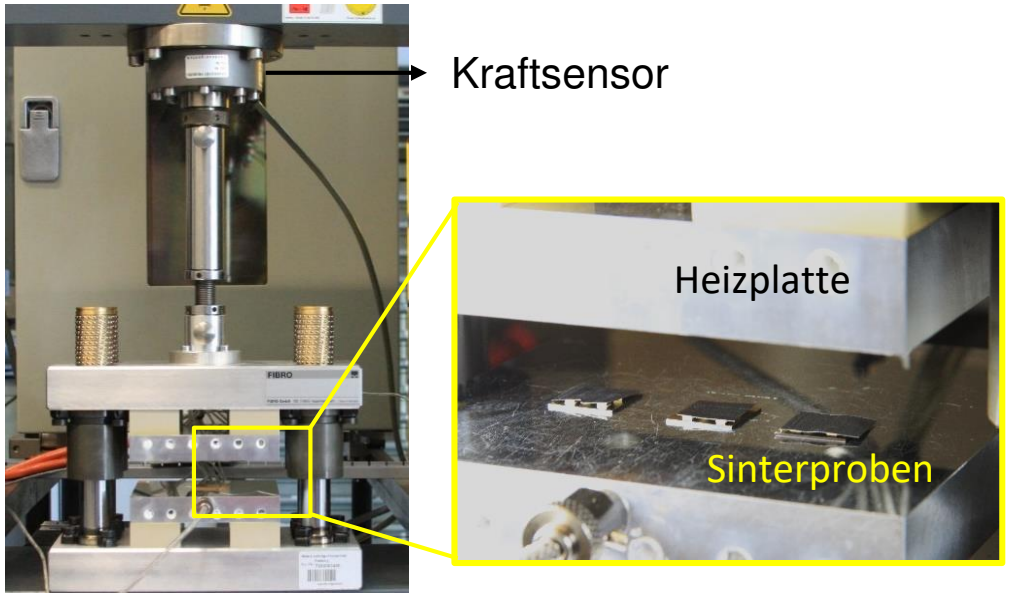




Herstellungsprozess für Silber-Sintern auf Nicht-DCB

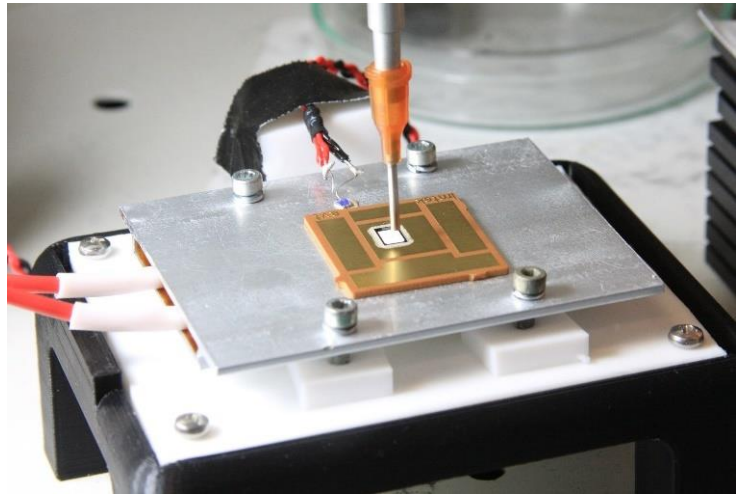
Sinterpresse

- Hochpräzise Kraftregelung via Zwick Z010
- Einzeln per PID-Controller regelbare Heizplatten (Thermisch vom Gehäuse entkoppelt)
- Gleichzeitige Verarbeitung mehrerer Substrate (Heizplattengröße: 120 x 120 mm²)



Prozessbedingungen

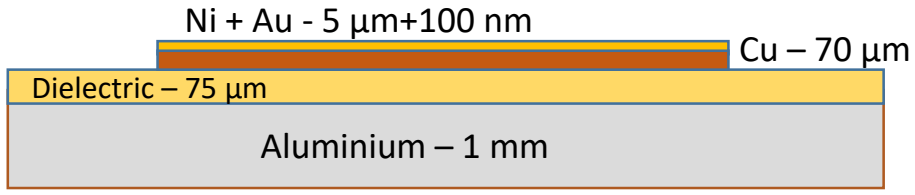
- Druck : 10 / 20 MPa
- Temperatur : 230 °C
- Zeit : 5 - 20 min
- Hot die placement



Materialien für die weitere Untersuchung (AIF Sinter)

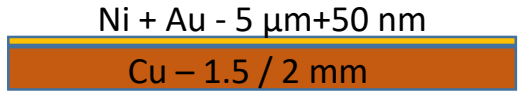
Substrat – Layout

IMS



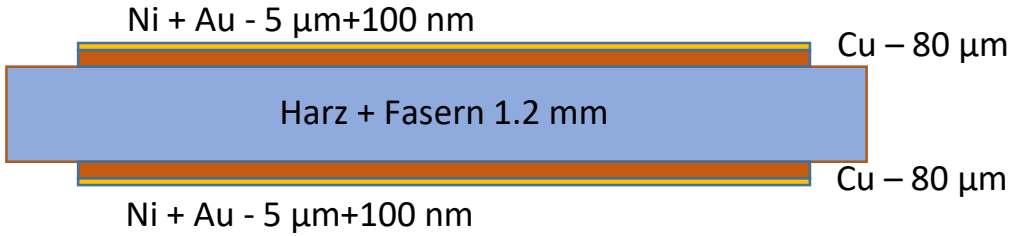
IMS (von *ts Leiterplattentechnik)*

Cu

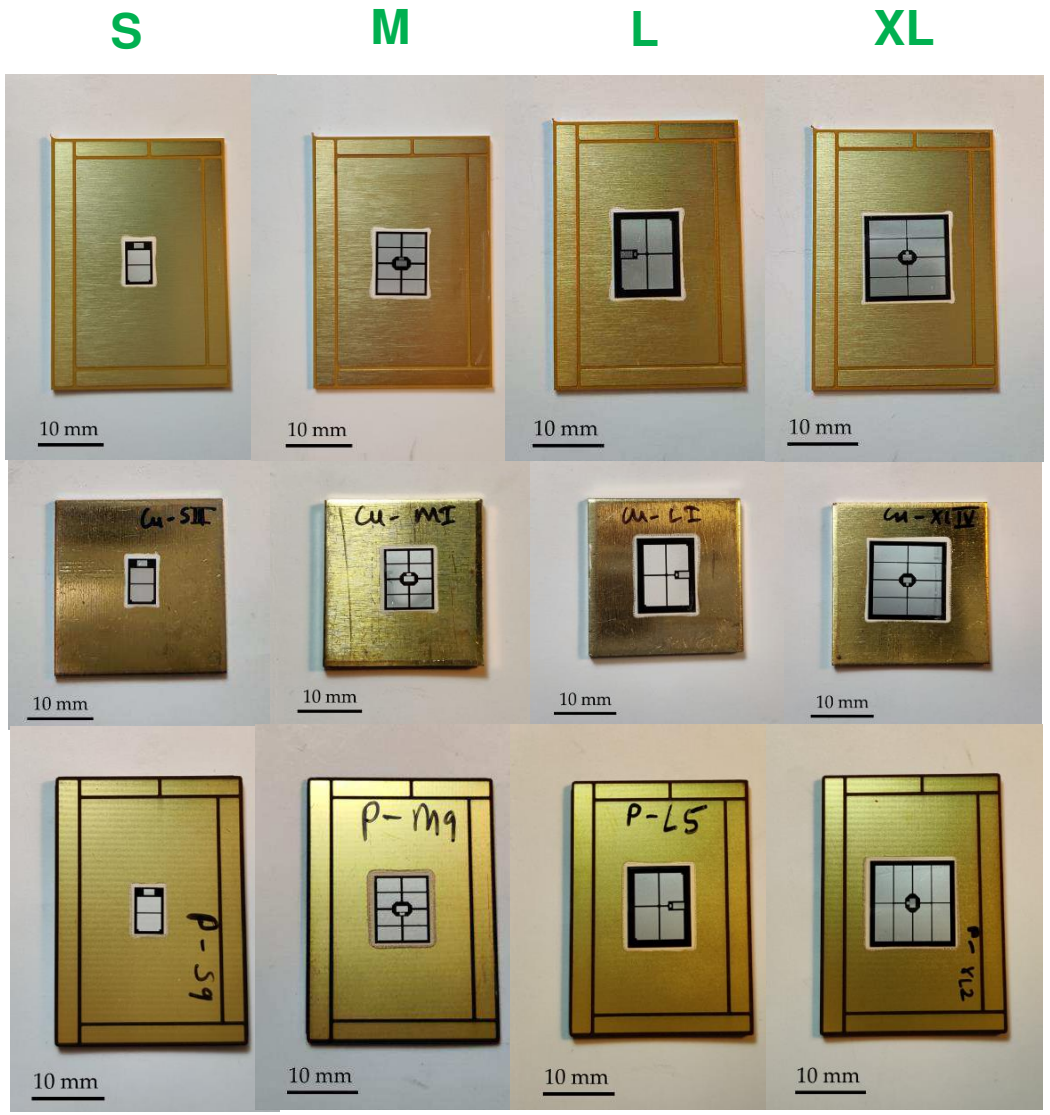


Cu *(Diotec Semiconductor AG)*

PCB



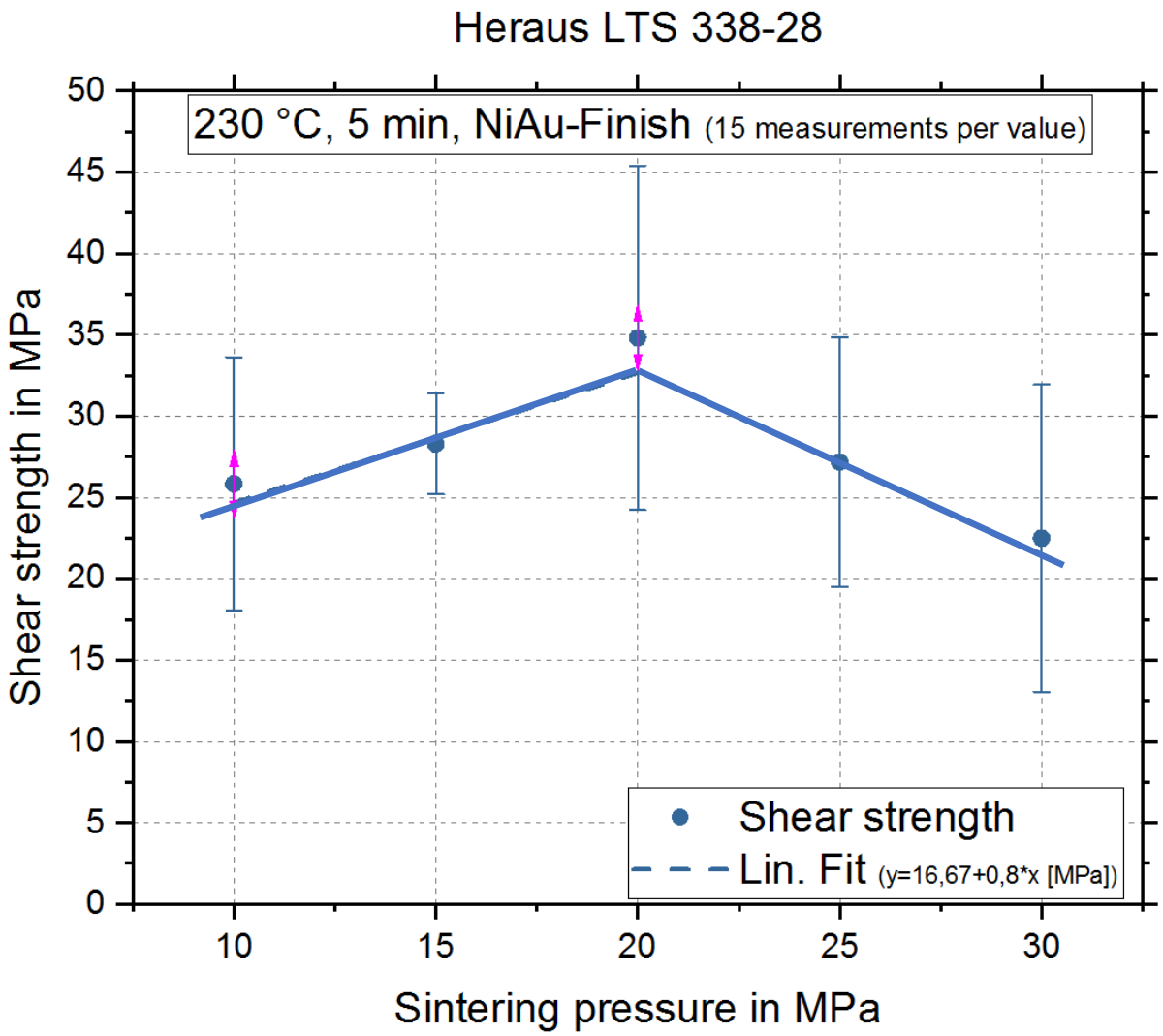
PCB Help-H (von *Schweizer Electronic AG)*



Process Development – Influence of the Sinter Pressure

Process and test conditions

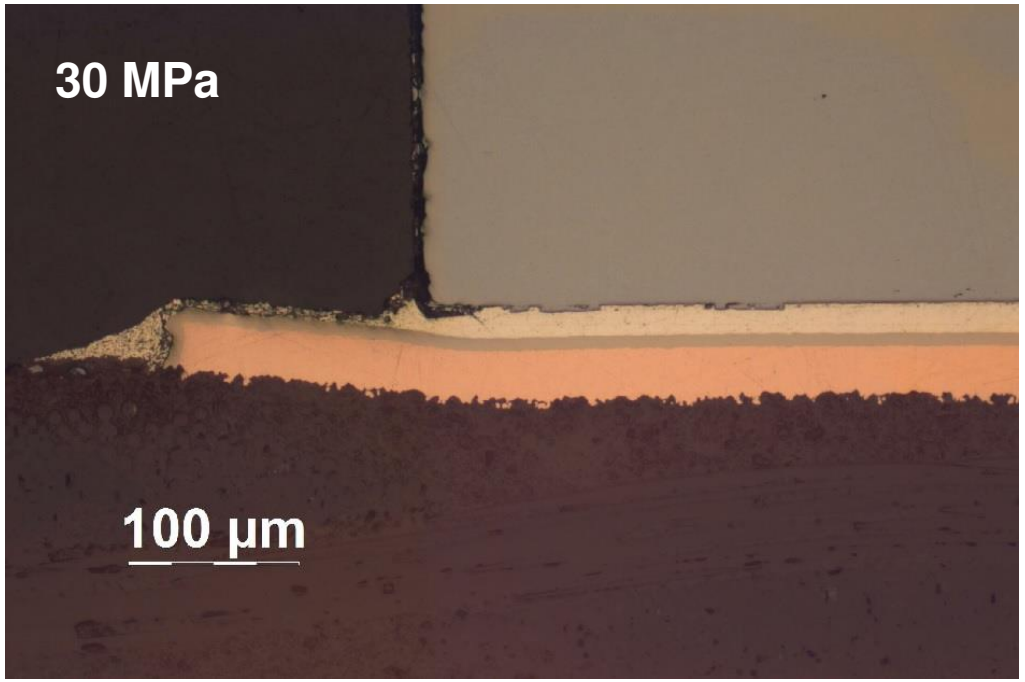
- 2x2 mm² Dummy-Chips, 3x3 Array
- Schweizer 2-layer PCB
  Isola IS550H
- 10 - 30 MPa, 230 °C, 5 min
- 2 Boards per pressure setting
- Shear-tests on 15 chips/set
- Cross-sections on 3 chips/set

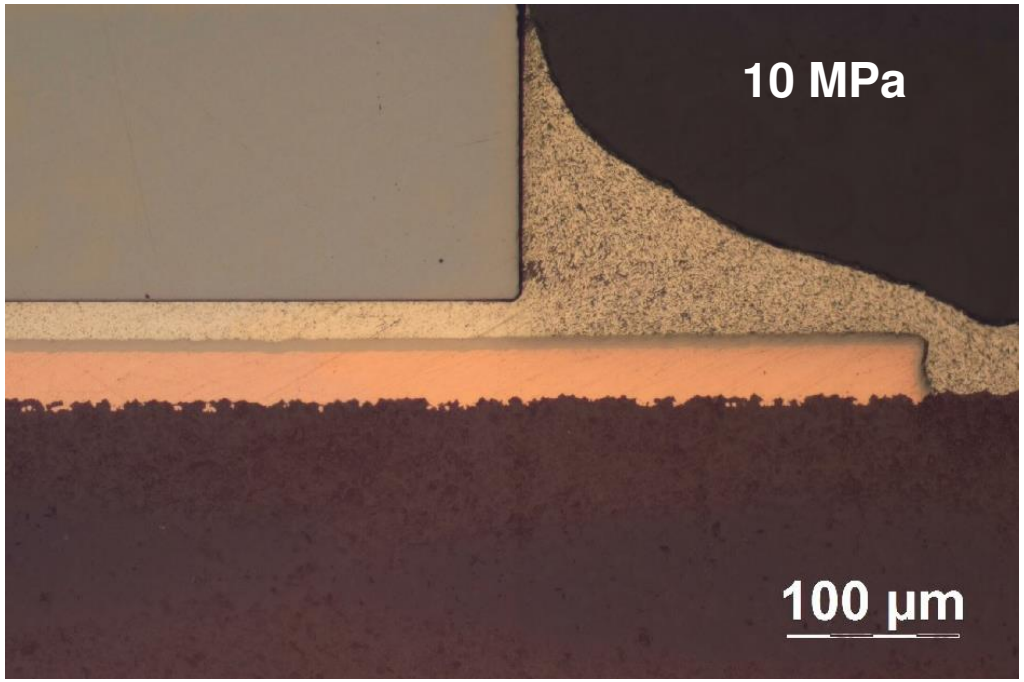


Sinterprozess-Entwicklung – Schädigung des PWB

Querschliffe der Sinterverbindungen

- 10 MPa Sinterdruck: Die Silberschicht hat noch Porosität.
- 30 MPa Sinterdruck: Eine dichte Silberschicht wird erzielt.
- 30 MPa Sinterdruck: Der Chip wird in die via-lose PWB gedrückt.

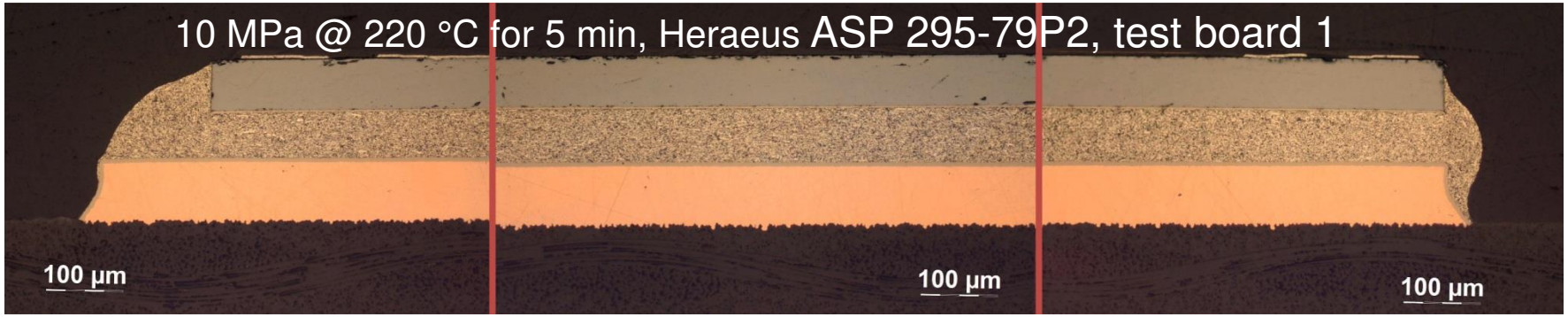


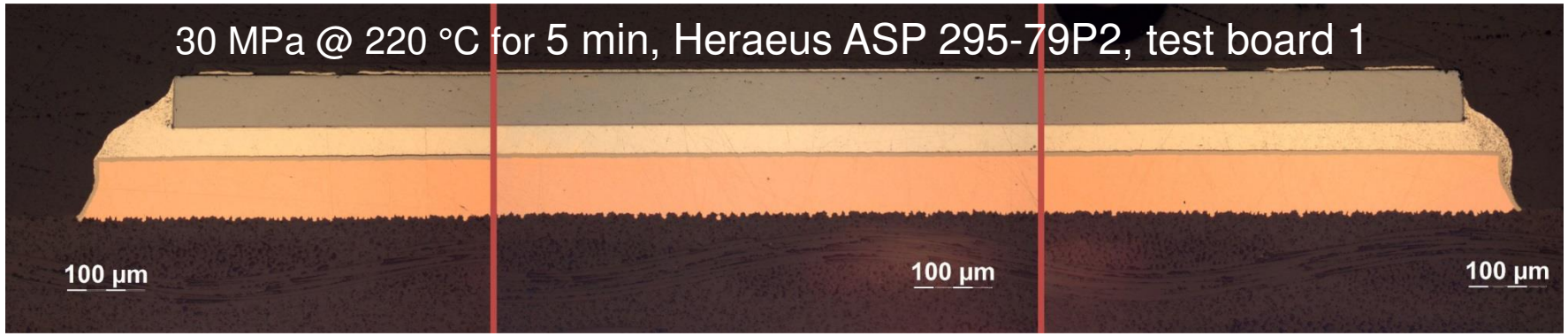


Sinterprozess-Entwicklung – Schädigung des PWB

Sintern auf thermischen Vias

- 10 MPa Sinterdruck: Die Silberschicht ist noch porös.
- 30 MPa: Die Silberschicht ist dicht; keine Schäden an PWB oder Chip



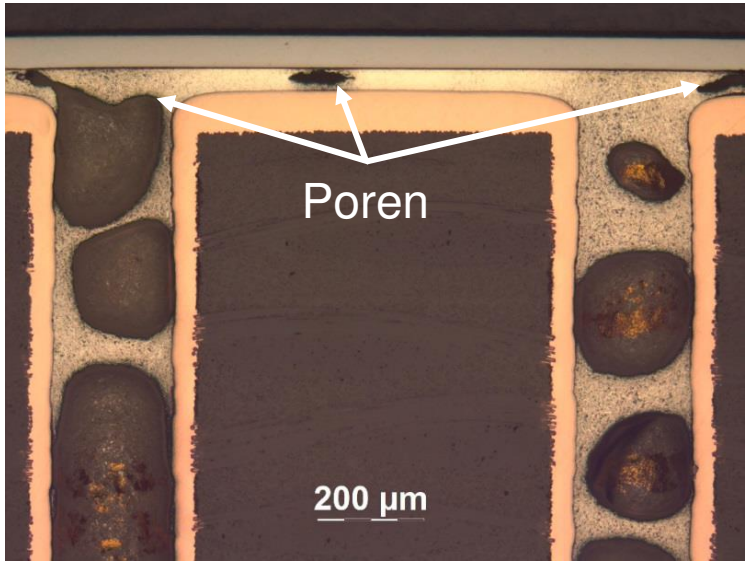


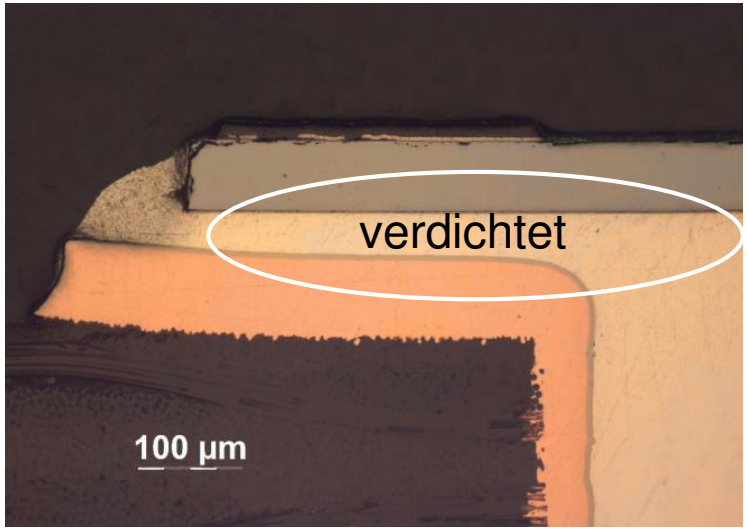
Sinterprozess-Entwicklung – Schädigung des PWB

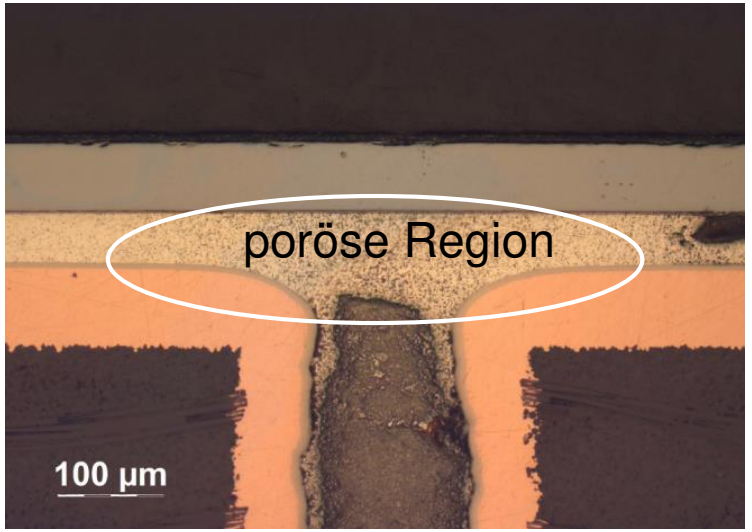
Querschliffanalyse der Sinterschicht an Vias

- 10 MPa @ 230°C für 5 min
- Heraeus ASP 295-79P2, Testboard 1
- Die Hohlräume der Vias enthalten Poren
- Poren auch im Umfeld

⇨ Abhilfe ggf. durch vorgefüllte Vias



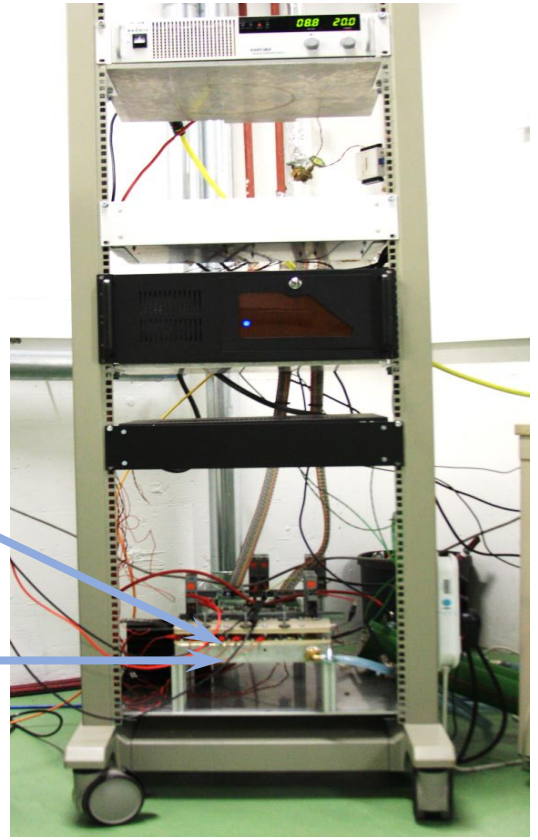




Zuverlässigkeits-Untersuchungen

Aktives Powercycling

- Aktives Zyklieren der Module
- Variable Testbedingungen:
  - Einstellen von ΔT_j =70 K bis 170 K
  - t_{on} =3 s und t_{off} = 6 s
  - Leistung = const., I_{CE}=70 A
- Ausfallkriterium
  - +5 % von V_{CE}
    +20 % von R_{th}



Power-Cycling-Anlage

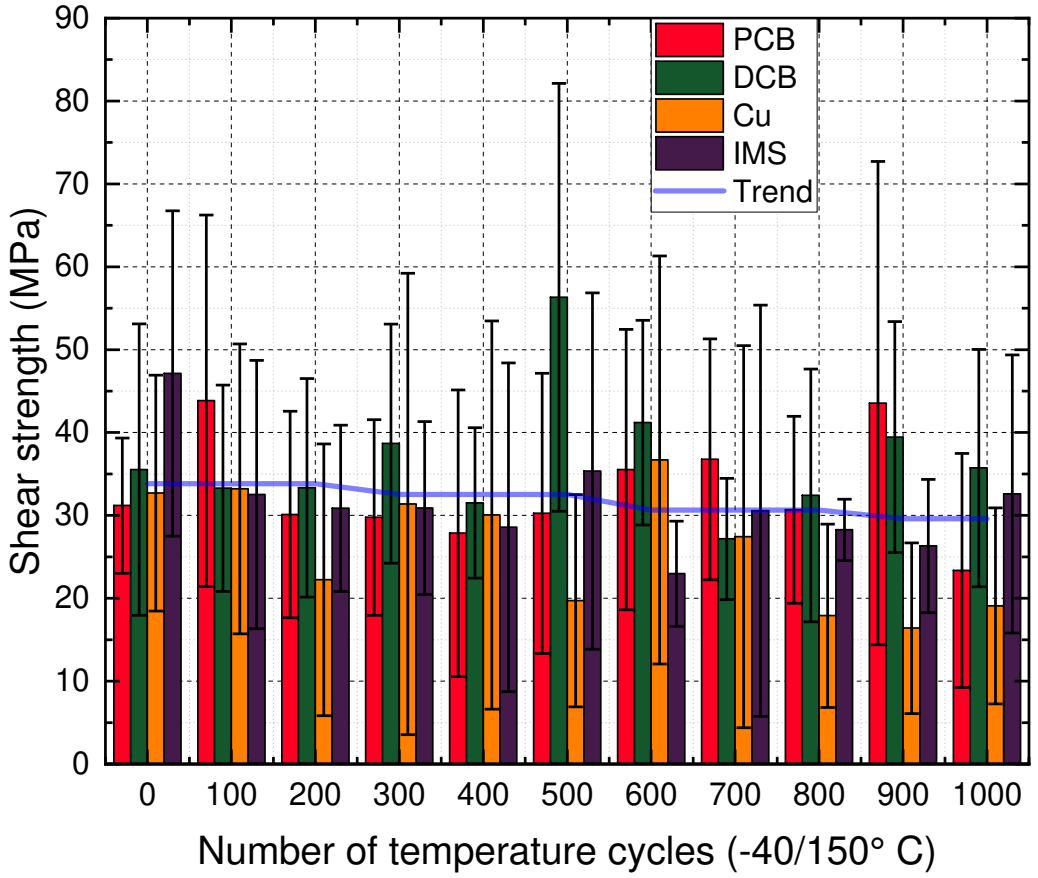
T-Schock-Anlage

Passive Zyklen, Temperaturschock

- Einfluss von Temperaturzyklen, -40/150 °C
- Parallele Untersuchung

AP4: Lebensdauertests
Scherfestigkeitsanalysen an 2*2 mm² Chips

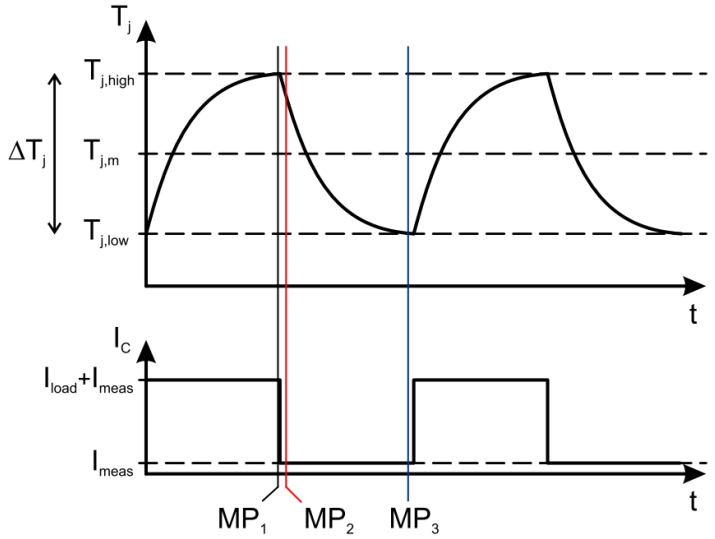
Probe	Scherfestigkeit in MPa (* interpoliert)		
	0 Zyklen	500 Zyklen	1000 Zyklen
PCB	31,2	30,2	23,4
DCB	35,5	42,3*	35,7
Cu	32,7	19,7	19,1
IMS	47,1	35,4	32,6



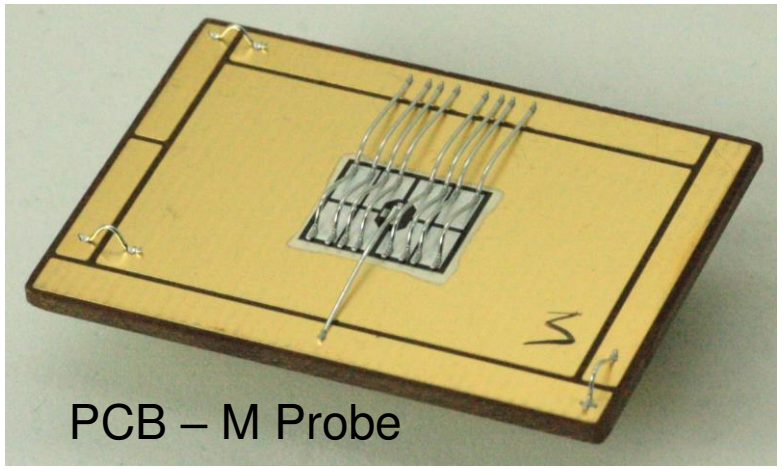
DCB > IMS > PCB > Cu

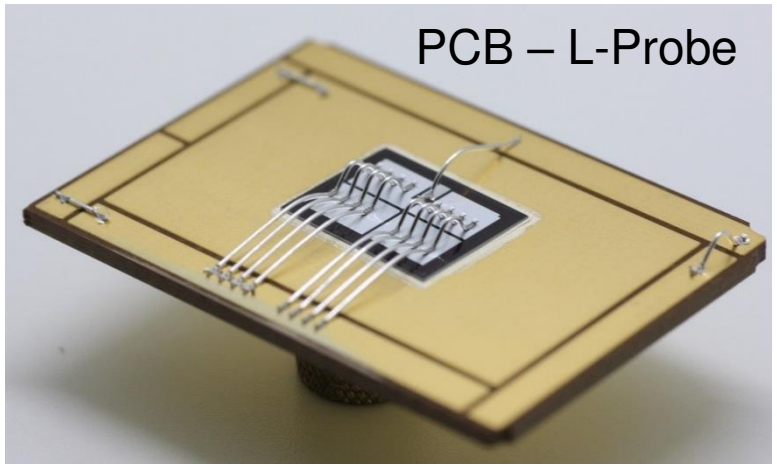
Lebensdauertests: Prüfstandmessungen

- Gemäß der Norm MIL-STD-883E muss $T_{j,max}$ zur Berechnung von $T_{j,max}$ nach dem Umschalten in die Kühlphase innerhalb von 100 µs aufgezeichnet werden



measuring point	measured quantity	calculated quantities
MP_1	V_{CEsat}	P_d $R_{th,jh}$
MP_1	T_h	$R_{th,jh}$
MP_2	V_{CE}	$T_{j,high}$ $R_{th,jh}$
MP_3	V_{CE}	$T_{j,low}$



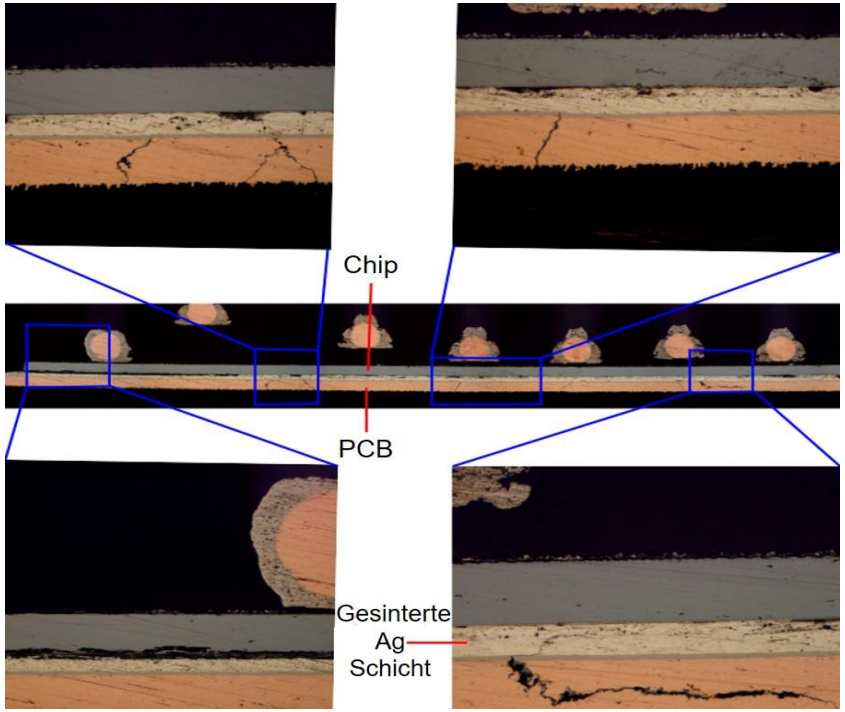


Injizierter Kollektorstrom, resultierende Sperrschichttemperatur und Messpunkte während des Zyklus

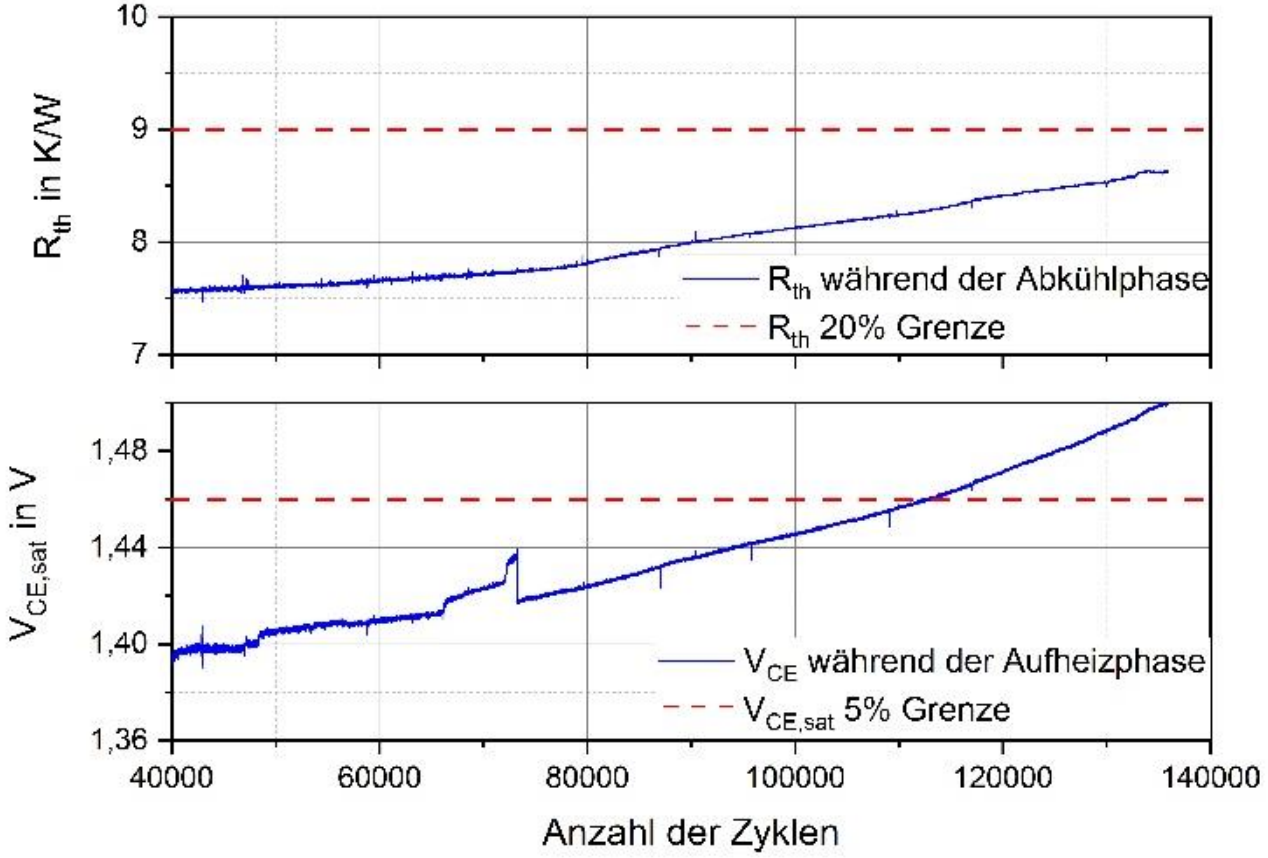
$$R_{th,jw} = \frac{T_{j,max} - T_w}{P_d} = \frac{T_{j,max} - T_w}{V_{CE,sat}(I_L + I_m)}$$

Lebensdauertests an PCB - S

- V_{CE}- und $R_{th,w}$ - Ergebnisse für aktive Lastzyklen
- V_{CE}-Versagenskriterien bei 113.000 - Zyklen erreicht
  - PCB- Help H Proben mit IGBT (6,57 x 4,2 mm²)
  - 20 MPa, 230 °C, 20 min



- ΔT_j = 163 °C
- t_{on} = 3 s / t_{off} = 6 s



Active Power Cycle - Übersicht

Ausfallart: Gemischt: Bonddrahtabheber, Ermüdung in Leiterplatte

Muster	ΔT_j in °C	I_L in A	t_{on} in s	t_{off} in s	Anzahl der Zyklen
PCB-S	159	20	3	6	129.960
PCB-M	151	32	3	6	163.181
PCB-XL	131	37	3	6	176.274
PCB-L	152	31	3	6	~202.690
DUT 5 DCB	**150**	**200**	**1,5**	**3**	**~95.000**

DUT1 - DUT4 = IS550H-PCB + IGBT (6,57 x 4,2 mm²)
DUT5 = DCB – Bondbuffer mit Grundplatte

Wirkung von Einflussgrößen auf Lebensdauer N_f

- Temperatur ⇩
- Dicke des Chips ⇩
- Größe des Chips ⇩
- Porosität ⇩
- Dicke der Sinterschicht ⇧

- Substrat CTE & *E* ⇩
  1. PCB
  2. IMS
  3. Cu

→ **In der Reihenfolge der Leistung geordnet**

Dicke des Chips >> Größe

$$N_f = C_1 \cdot \left[\left(\alpha_S T_S - \alpha_C T_C \right) \cdot \sqrt[3]{E_C \cdot E_S \cdot E_{Ag}} \cdot \sqrt{\frac{l_C}{d_{Ag}}} \right]^{C_2}, C_2 < 0$$

Klett-Welding with Nano-Wires

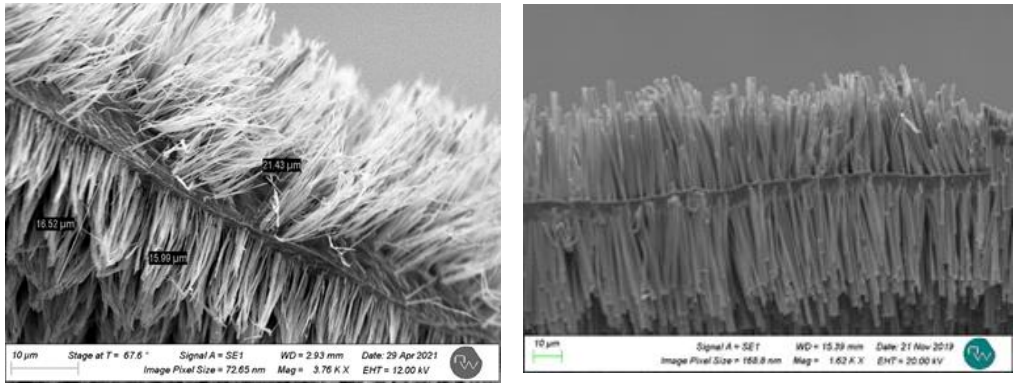
Pure copper sheet with electro-chemically deposited NanoWires

Current standard design and process

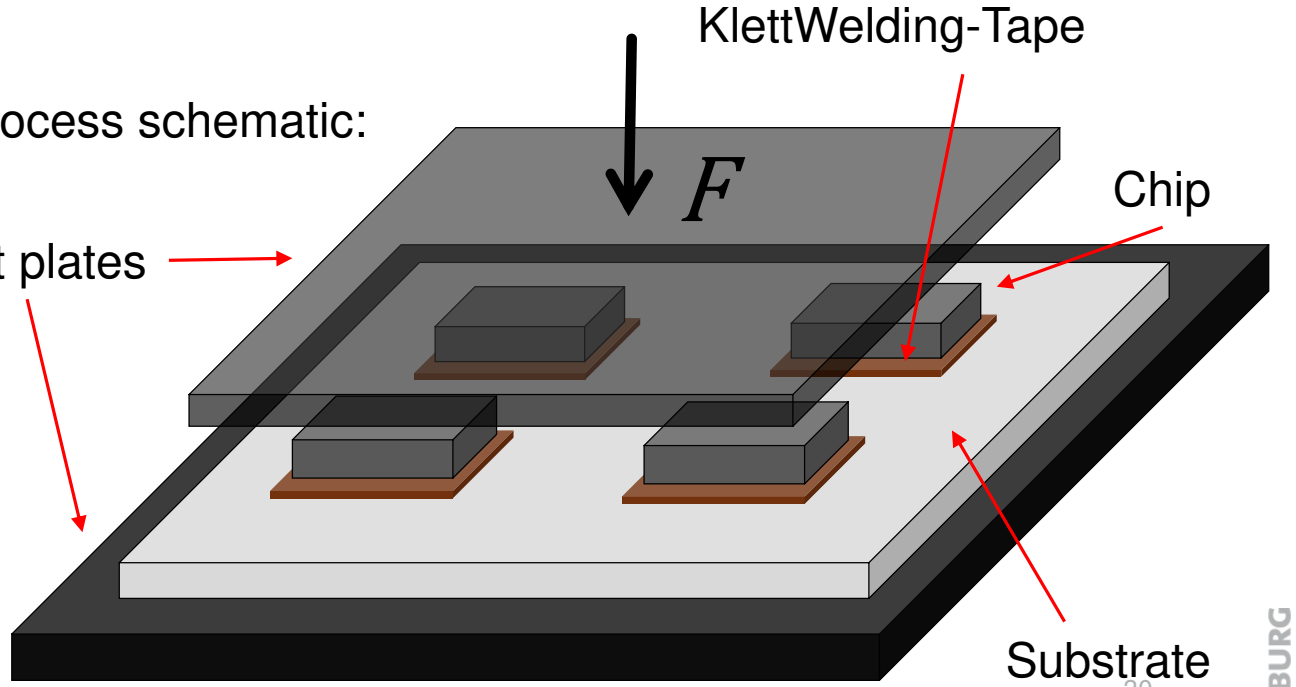
- 20 µm copper core sheet
- 45 µm wire length, 1000 nm diameter
- Sintering @230 °C with 20 MPa pressure for 120 s

Possible Parameters	Upper Limit	Lower Limit
Wire diameter	1000 nm	100 nm
Wire length	50 µm	10 µm
Wire density	20 %	30 %

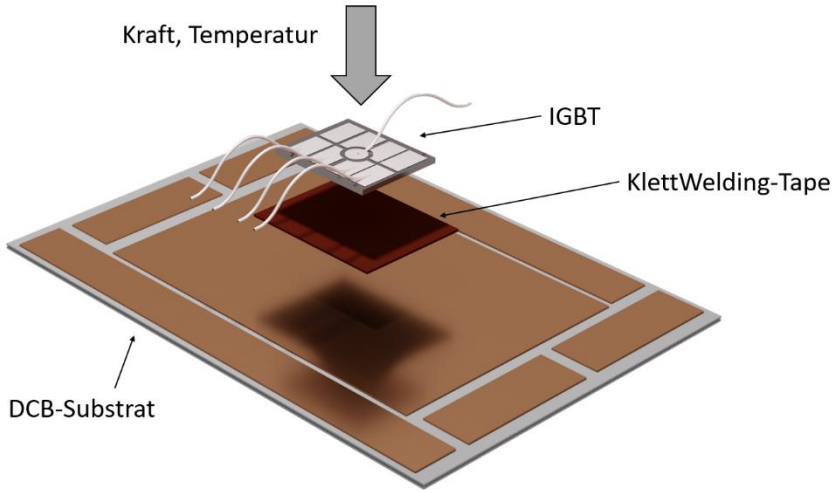
SEM-images

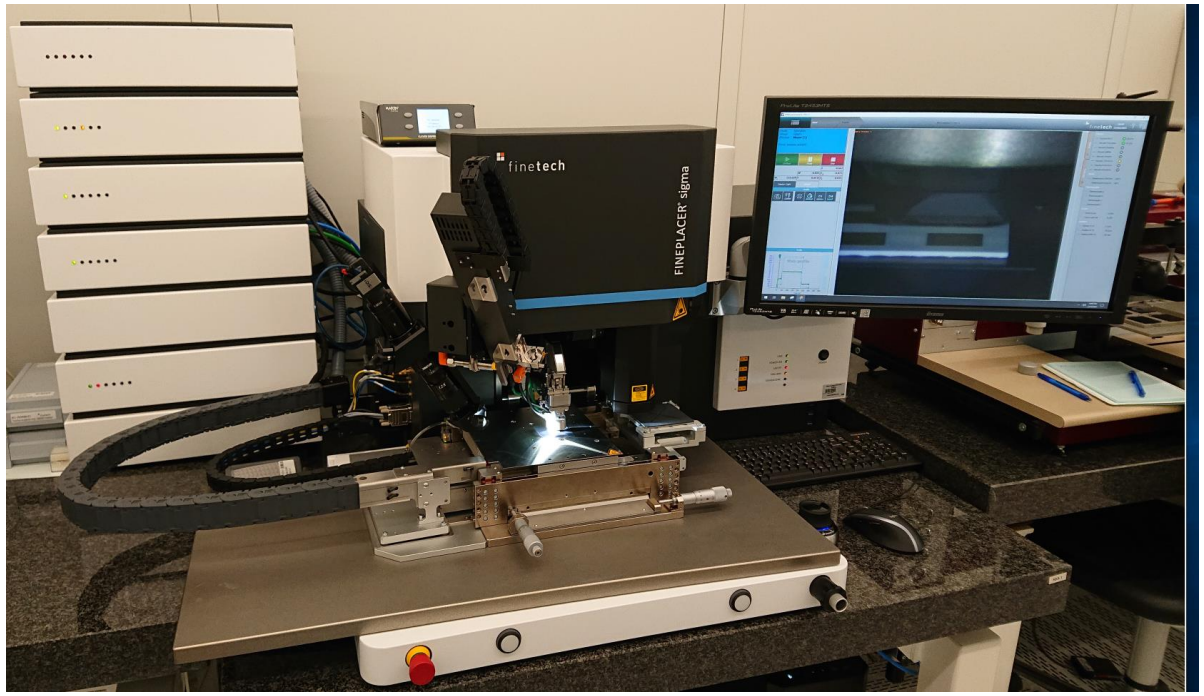


Process schematic:



Klett-Welding with Nano-Wires: Results of ZIM-Project





Optimum parameters	
Diameter	100 nm
Length	25 µm
Pressure	15- 20 MPa
Temperature	180 °C
Sintering time	120 s
Atmosphere	N_2

Specimens	Surface	Roughness R_a
Test chips	2 x 2 mm^2 Si (50 nm Ti, 100 nm Ni, 200 nm Ag)	3.4 nm
DCB	Bare copper finish (300 µm Cu)	2.3 µm

Klett-Welding with Nano-Wires

Sinter time

- Metallographic cross-sections
- Measurement of the electrical resistance during sintering

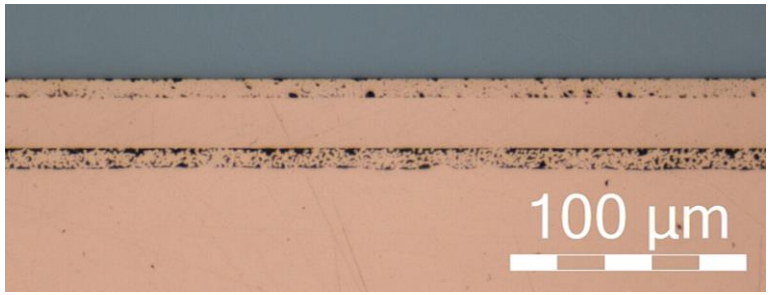
Sinter pressure

- Systematic variation from 12 to 30 MPa

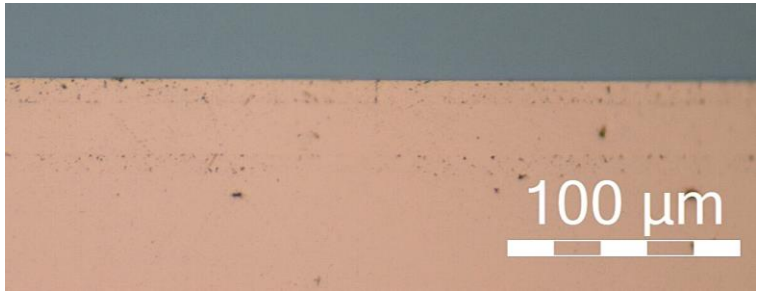
Sinter temperature

- Systematic variation from 210 °C to 170 °C

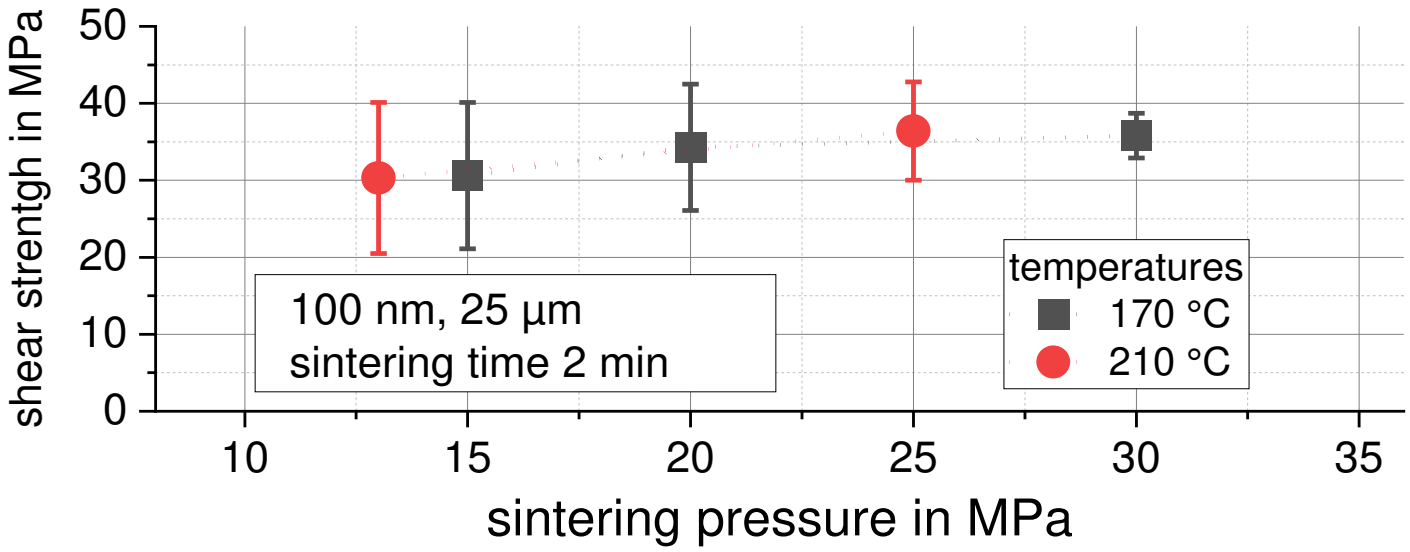
Shear testing



10 s sintering time



120 s sintering time



Klett-Welding with Nano-Wires

Wire diameter varied:

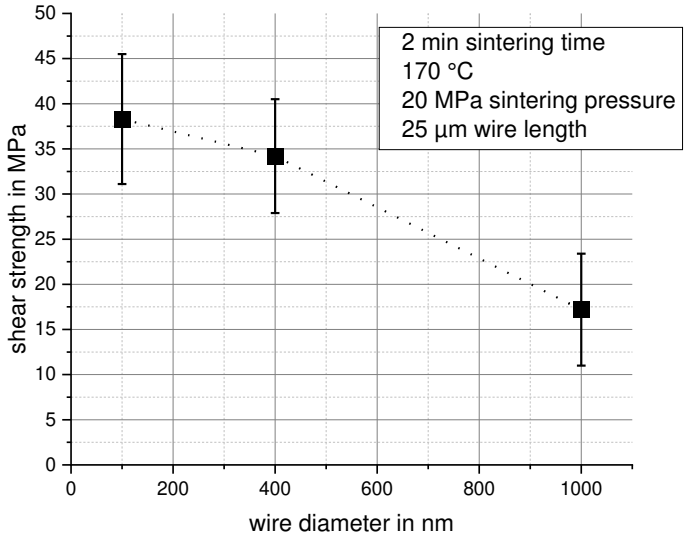
- 100, 400, and 1000 nm

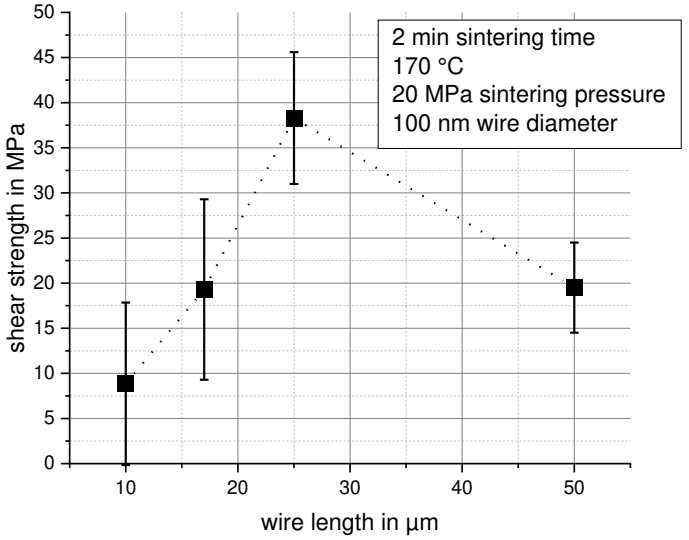
Wire length varied:

- 10, 20, 25 and 50 µm

→ Significant increase in shear strength with lower diameter due to higher surface/volume ratio

→ optimum length of 25 µm



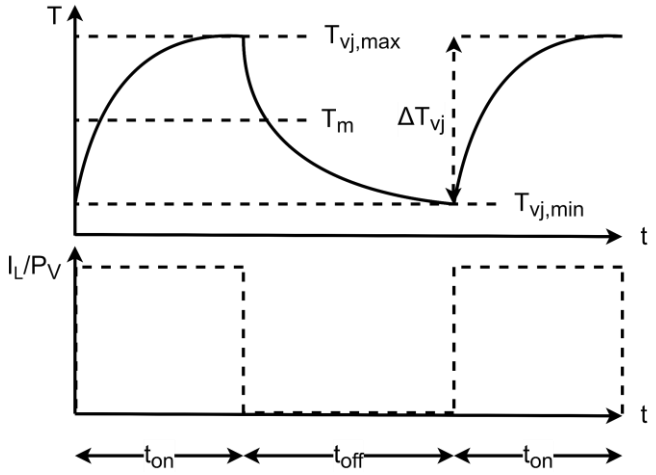


Chosen tapes for further experiments and lifetime testing

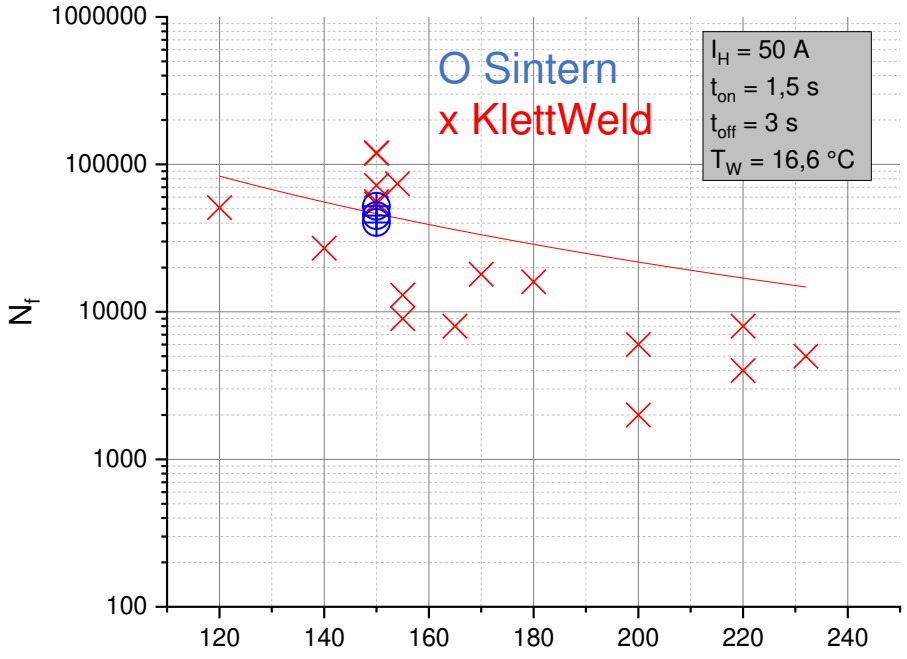
Tape-No.	Diameter	Length	Density
100	100 nm	25 µm	30 %
400	400 nm	25 µm	30 %

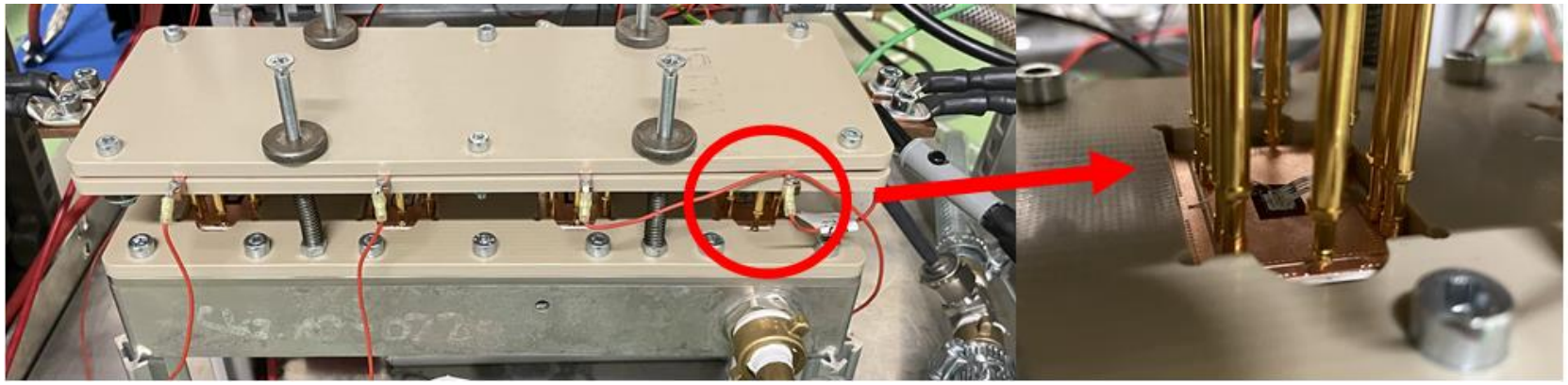
Klett-Welding with Nano-Wires – Power Cycling

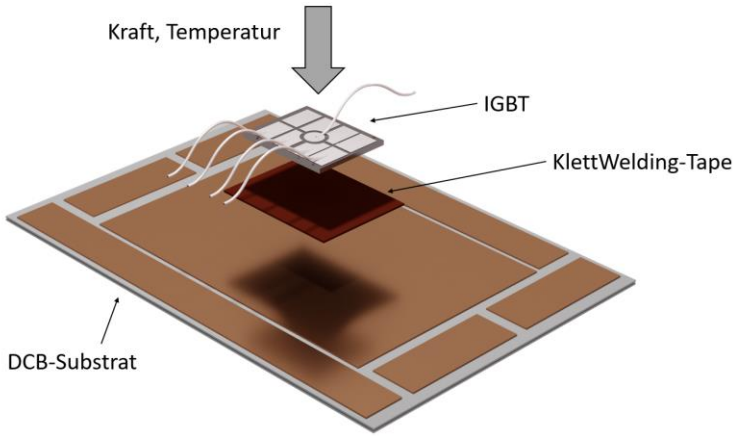
Active Power Cycling Test (APCT)



Infineon IGC28T65T8M IGBT	
U_{CE} and I_C	650 V; 50 A
Size	6,6 · 4,2 mm²
Thickness	80 µm
ΔT in K	90 - 200
t_{on} / t_{off}	1,5 / 3 s







Evaluation von neuen Bondverfahren

Eigenschaft	ICA Kleben	Ag-Sintern	AgSn-TLP	Cu-Klett-Welding	PbSn-Löten
Prozesskomplexität	++	o	o	o	+
Niedrige Bondtemperatur	++	+	+	++	o
Bondstabilität	+	+	+	+	+
Thermische Leitfähigkeit	o	++	+	++	+
Höchstleistungs-Module	o/+	++	++	++	++
Toxizität/Umwelt	+	+	+	+	--
Prozesskosten	+	o	o	+	+
Prozessverfügbarkeit	++	+	o	o	++
Materialverfügbarkeit	++	++	-/o	+	++

LowTemp-TLP (AiF – IGF)

Forschungsthema:

- Schonendes TLP-Fügeverfahren bei Prozesstemperaturen unter 150°C durch Anwendung ternärer Systeme (LowTemp-TLP)

Laufzeit 30 Monate:

- 01.05.2021 – 30.11.2023

Forschungseinrichtungen:

- Hahn-Schickard-Gesellschaft für angewandte Forschung e.V. (FV)
- fem, Forschungsinstitut Edelmetalle + Metallchemie
- Albert-Ludwigs-Universität Freiburg, IMTEK - AVT

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- **an unsere Partner,**
- **für die Förderung!**

Diotec Semiconductor

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Heraeus