

LTS - Low temperature soldering Niedrig schmelzende Lote in der Elektronikfertigung

Helge Schimanski
Fraunhofer ISIT

Hans-Juergen Funke
Nexperia Germany GmbH



© Fraunhofer ISIT

1

Fraunhofer ISIT

Forschungs- und Entwicklungszentrum für Mikroelektronik und Mikrosystemtechnik

- Forschungs- und Entwicklungszentrum für Mikroelektronik und Mikrosystemtechnik
- In Itzehoe seit 1995
- Erstinvestition: 125 Mio. €
- Gesamtinvest bis 2017: ca. 400 Mio. €
- Mitarbeiter: 150
- Zertifiziert nach ISO 9001:2015



- Institutsleiter: Prof. Dr. habil. Axel Müller-Groeling
- Vertreter: Prof. Dr. Holger Kapels

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022

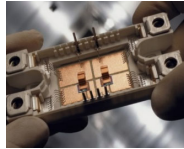


2

Fraunhofer ISIT Geschäftsfelder

- **Leistungselektronik**
Innovative Bauelemente
Elektronische Energiesysteme

Leistungsmodul

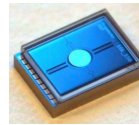
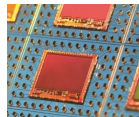


- **Batteriesysteme**
Fertigungstechnologie
Zellentwicklung
Batterieanalytik & Systeme

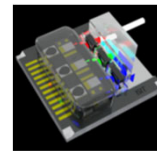
Maßgeschneiderte
Batteriezellen

- **MEMS-Anwendungen**
Optische Systeme
Akustische Systeme und Mikroantriebe
Agglomerierte Mikrosysteme

Mikrospiegel



Waferlevel-Packaging



Miniaturisierte RGB-LED

- **Mikro-Fertigungsverfahren**
Prozessintegration und Pilotfertigung
Modul-Services: QZ und AVT

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



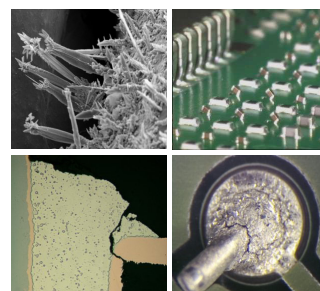
Fraunhofer
ISIT

3

Modul-Services – Qualität, Zuverlässigkeit und AVT elektronischer Baugruppen und Komponenten

Fortschrittliche Fehleranalyse ist die Grundlage für Innovation, Geschwindigkeit, Qualität, Zuverlässigkeit und garantierte Funktion über Lebensdauer

- Material- und Schadensanalysen, Kontaminations-, Korrosions- und Rückstandsuntersuchungen
- Bewertung der Herstellungsqualität nach Industriestandards
- Zuverlässigkeits- und materialkundliche Bewertung
- Einführung neuer Technologien
- Prototyping und Vorserienfertigung
- Prozessoptimierung, Bauteil- und Materialqualifizierung (Lötwärmebeständigkeit, Lotpastenbewertung, u.a.)
- Rework komplexer Baugruppen
- Seminare und In-House-Schulungen



Whisker-, Tombstone- (oben) und Rissbildungen (unten) an elektronischen Bauelementen



ISIT SMT-Testbord

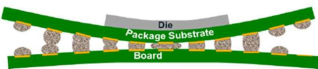
All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022




Fraunhofer
ISIT

4

Wölbung BGA

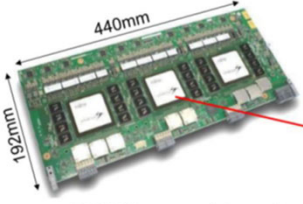




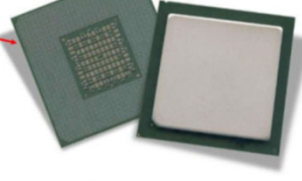
SPARC64™ XIfx outline (2014)

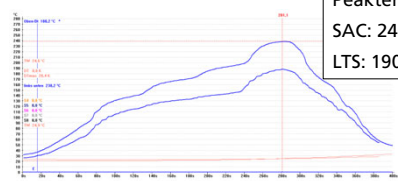
First Full LTS BGA product

- Chip Size : 25.8x28.0mm
- PKG Size : 63.0 x 63.0 x 5.14mm
- BGA : **4,384**pin **0.8mm**Pitch
- Signal : 996pin

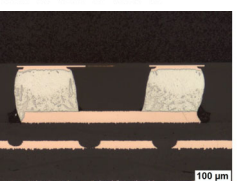
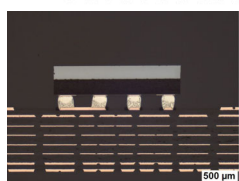


CPU Memory Board





Peaktemperature:
SAC: 240°C
LTS: 190°C




CTE unterschiedlich, Lötwärme im SAC-Reflowprozess führt zu offenen Lötstellen

Abhilfe: Low Temperature Soldering (SnBiX), nur möglich wenn Mission Profile passt











All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.

© Fraunhofer ISIT 2022.




5

Package Selection Representing Nexperia Package Portfolio

Package Platforms	Lead finish technology	Representative packages
 Small-signal Medium-power Power Small-signal flat lead	Leadframe variants: NiFe with Cu plating Cu alloy leadframe Lead finish: matte Sn plating, thickness 10...20µm	SOT363  2.0x2.0mm²
 DFN DQFN DFN2111-7 X2SON	Leadframe: Cu alloy with NiPdAu plating Pad finish: matte Sn plating, thickness 10...20µm or NiPdAu	DFN1010B-6  1.0x1.0mm² DFN1110D-3  1.1x1.0mm²
 LPAK family Gullwing CFP family	Leadframe: Cu alloy Lead finish: matte Sn plating, thickness 10...20µm	LPAK56  5.0x6.0mm²
 DSN1608-2 DSN0402-2 WLCSP15 WLCSP4	Variants: WLCSPs with SAC solder balls DSN with Cu contacts (8µm) and Sn plating (3µm) DSN with NiAu contacts	DSN0603  0.6x0.3mm² WLCSP12  1.4x1.9mm²

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.

© Fraunhofer ISIT 2022.



6

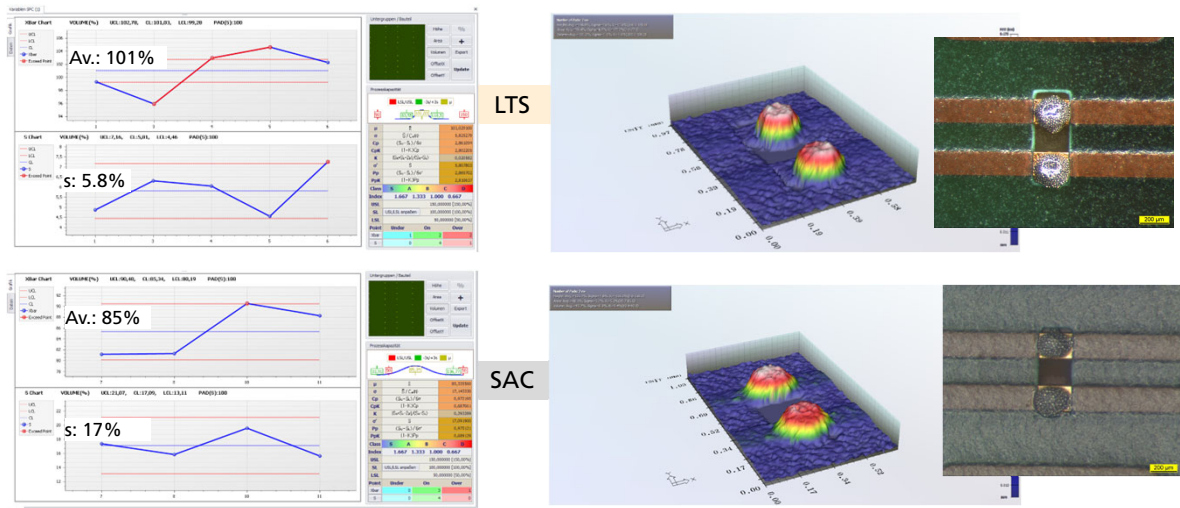
Solder Paste Printing

- Solder pastes
 - LTS: SnBiX, Melting point: 138-142°C, ROL0, T4
 - SAC: SAC305, Melting point: 217-219°C, ROL0, T4
- Stencil
 - Stainless steel, brushed, coated, 80µm, 100µm, 120µm

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



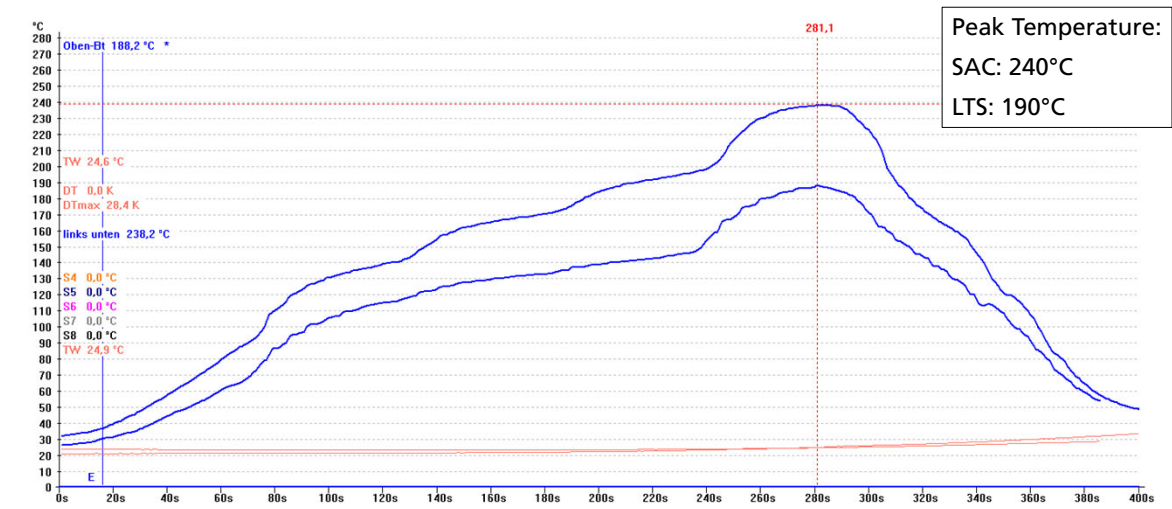
Solder Paste Inspection (SPI) DSN0603



All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



Reflow Profiles According Datasheet of Solder Pastes



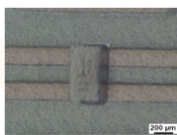
All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022.



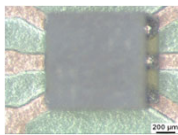
9

Optical Inspection after soldering

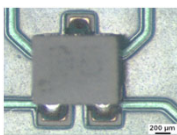
LTS



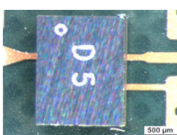
DSN0603



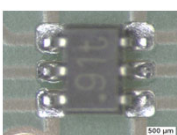
DFN1010-6



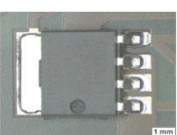
DFN1110D-3



WLCSP12

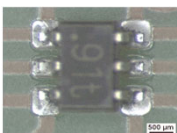
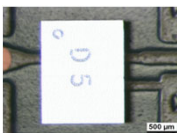
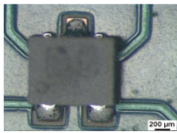
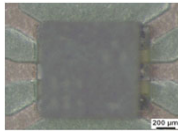
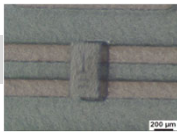


SOT363



LPAK56

SAC



■ No difference between LTS and SAC

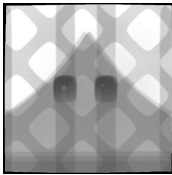
All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022.



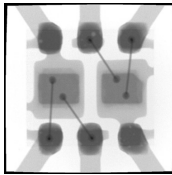
10

Xray Inspection

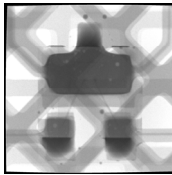
LTS



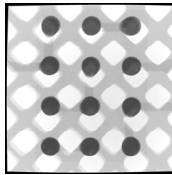
DSN0603



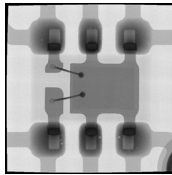
DFN1010-6



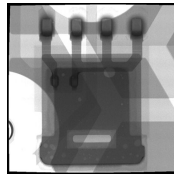
DFN1110D-3



WLCSP12

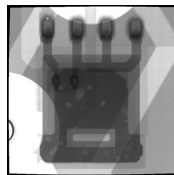
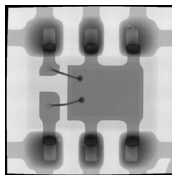
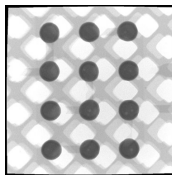
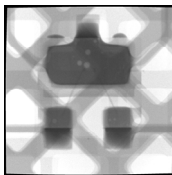
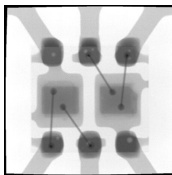
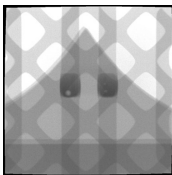


SOT363



LFPAK56

SAC



All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022

Tilting and component height of BTC and WLCSP12

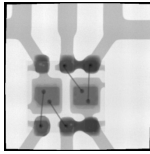
Solder	LTS				SAC			
	Max. Tilting angle		Max. height difference	Mean height	Max. Tilting angle		Max. height difference	Mean height
Package	long side	short side			long side	short side		
DSN0603	0.6	15.2	77	336	2.2	15.3	70	336
DFN1010-6	2.8	0.4	56	358*	0.7	2.2	42	385*
DFN1110D-3	0.4	4.6	61	505	0.3	4.1	65	505
WLCSP12	0.5	0.8	19	556**	0.3	0.2	26	532**

No significant difference between LTS and SAC, except:

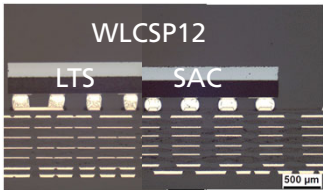
* Difference due to solder volume (bridging) with LTS

** Difference due to incomplete melting of SAC ball

DFN1010-6



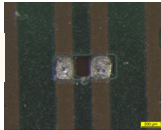
WLCSP12



All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022

Shear strength, view to remains on PCB

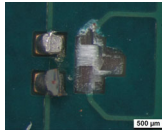
LTS



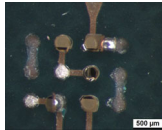
DSN0603



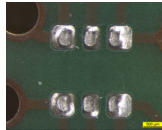
DFN1010-6



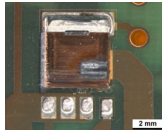
DFN1110D-3



WLCSP12

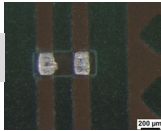


SOT363

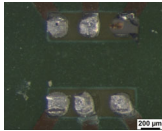


LFPAK56

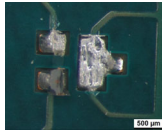
SAC



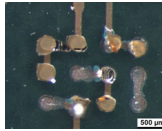
DSN0603



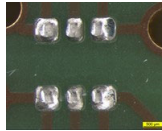
DFN1010-6



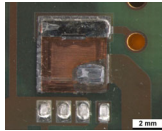
DFN1110D-3



WLCSP12



SOT363



LFPAK56

- No difference in shear mode between LTS and SAC (0c as well after 1500 cycles)
- Crack in solder are as well visible as torn out PCB pads and broken package housings

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



13

Shear strength comparison, TCT -40°C/+85°C , 0c vs 1500c

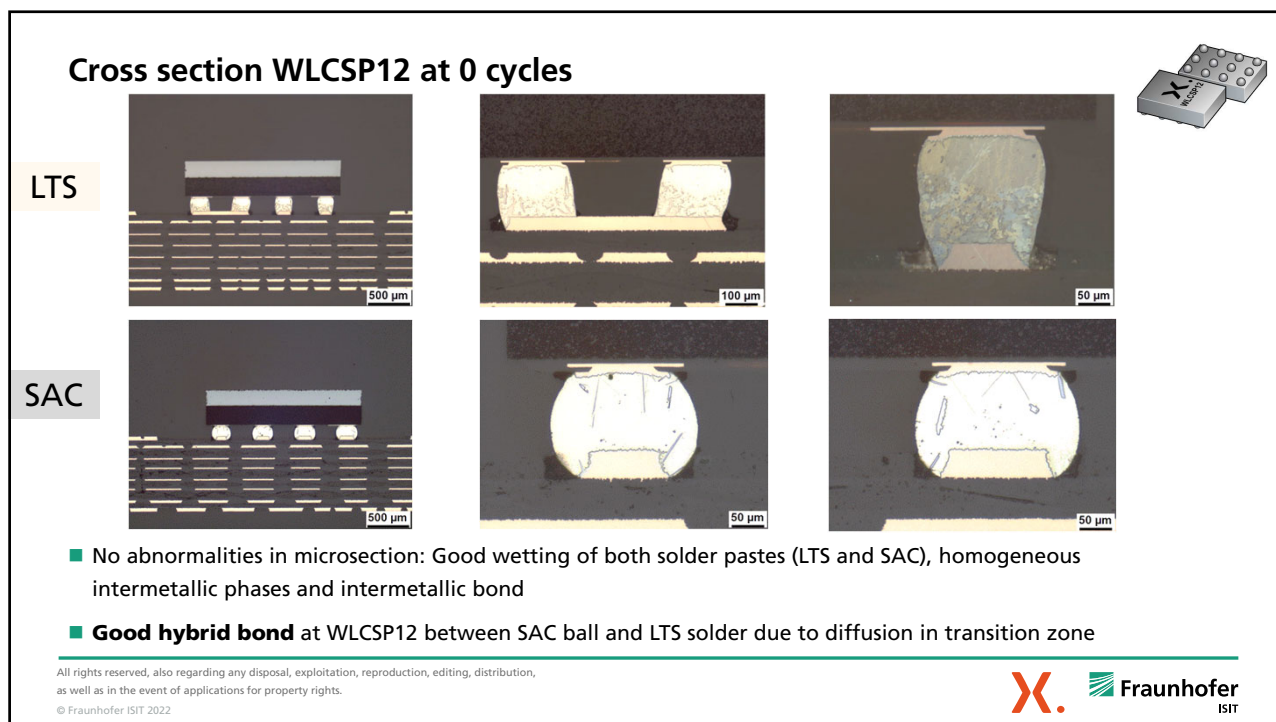
Package	Shear Strength [N/mm²]				Shear Mode
	0 cycles		1500 cycles		
	LTS	SAC	LTS	SAC	
DSN0603	73.37	68.87	61.29	60.82	Solder joint
DFN1010-6	77.12	72.37	76.08	65.06	Solder joint / Package
DFN1110D-3	42.51	36.57	40.67	34.05	Solder joint / Package / PCB
WLCSP12	30.16	32.52	32.48	31.21	Package / PCB
SOT363	44.08	29.27	36.43	28.33	Solder joint
LFPAK56	18.35	14.36	17.53	15.04	Package

- Shear strength fulfill industry established limit of 20N/mm², even after TCT, except LFPAK56
- For LFPAK56 shear mode is package breakage due to large heatsink which result in very solid solder connection: shear force values ~30Kg which confirms package and solder joint is very robust for applications
- Acceptable shear strength degradation after TCT, except WLCSP12 (value is within spread of measurement)
- Shear strength is higher using LTS, because of higher mechanical material strength

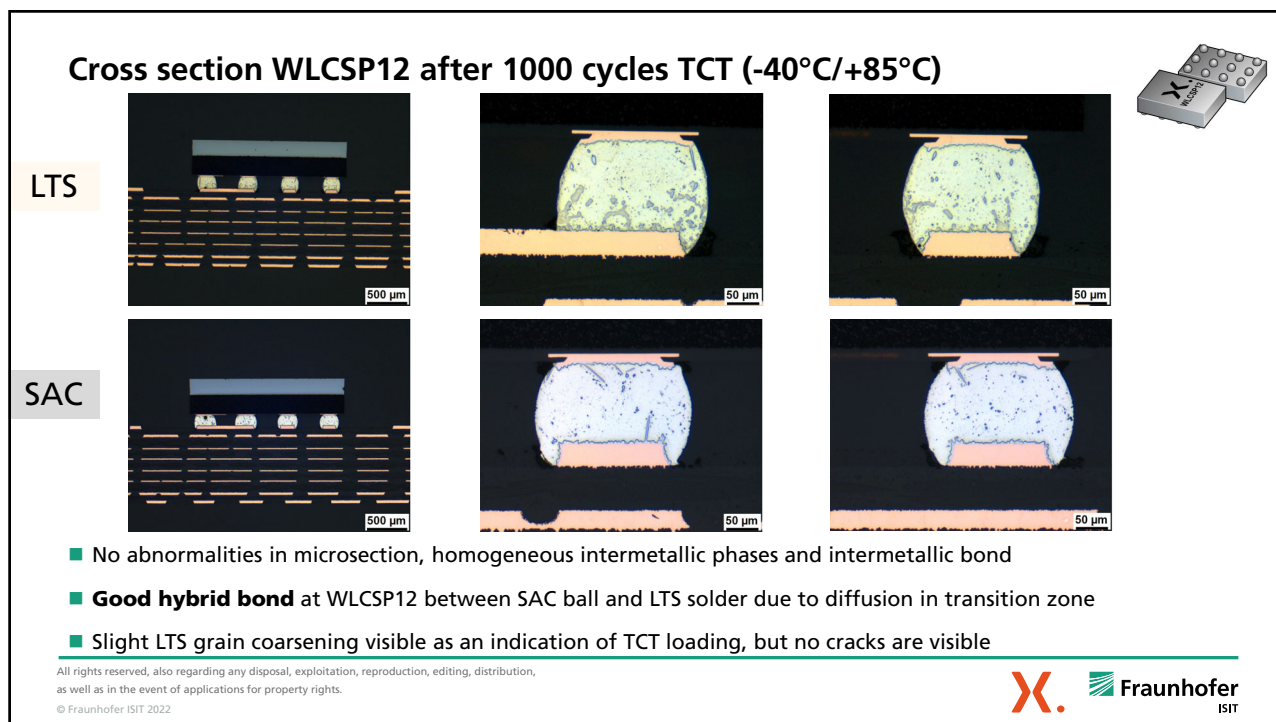
All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



14



15

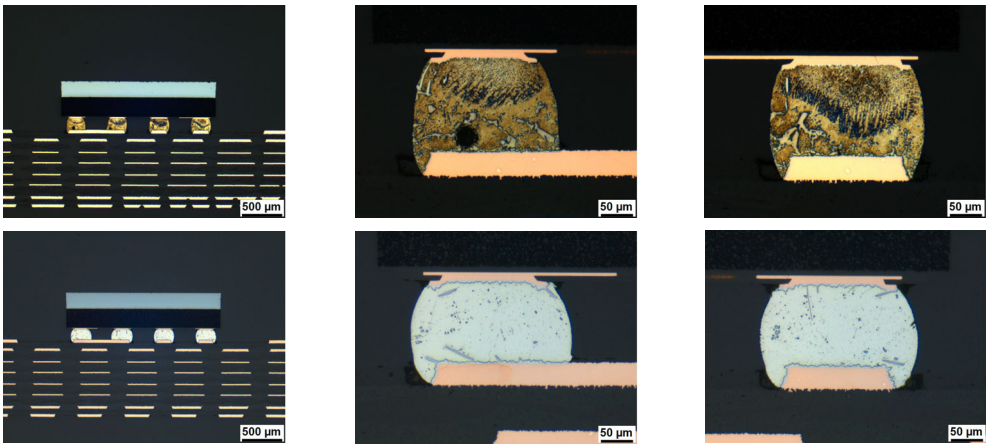


16

Cross section WLCSP12 after 1500 cycles TCT (-40°C/+85°C)


LTS


SAC




- No abnormalities in microsection, homogeneous intermetallic phases and intermetallic bond
- Good hybrid bond** at WLCSP12 between SAC ball and LTS solder due to diffusion in transition zone
- LTS grain coarsening visible as an indication of TCT loading, but no cracks are visible
- Discolouration of LTS solder due to etching

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022





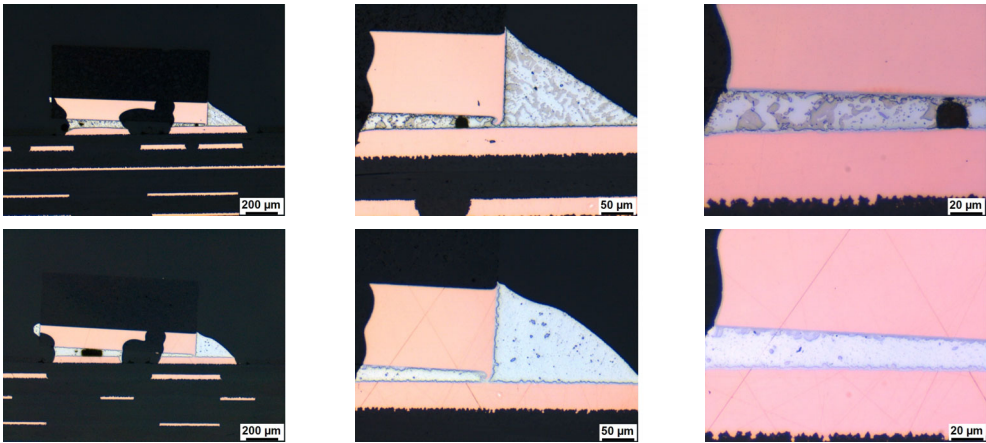


17

Cross section DFN1110D-3 after 1500 cycles TCT (-40°C/+85°C)


LTS


SAC




- LTS and SAC, homogeneous intermetallic phases and intermetallic bond
- LTS grain coarsening visible as an indication of TCT loading, but no cracks are visible

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022







18

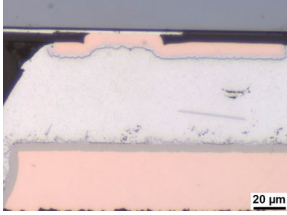
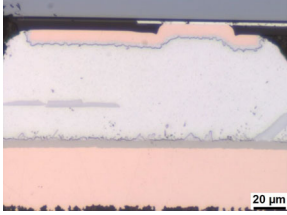
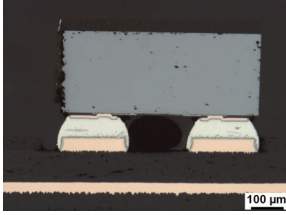
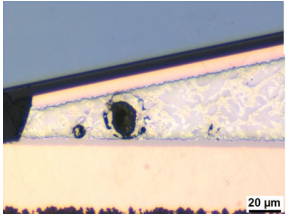
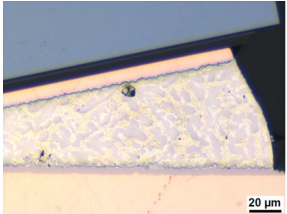
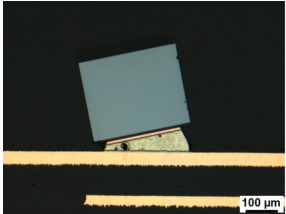
Helge Schimanski, Fraunhofer ISIT
LTS - Low temperature soldering

9

Cross section DSN0603 after 1500 cycles TCT (-40°C/+85°C)

LTS

SAC



■ LTS and SAC, homogeneous intermetallic phases and intermetallic bond

■ LTS grain coarsening visible as an indication of TCT loading, but no cracks are visible

■ Discoloration of LTS solder due to etching

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.

© Fraunhofer ISIT 2022

X.

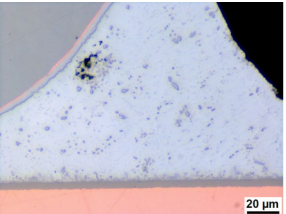
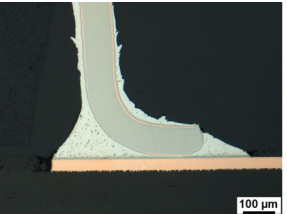
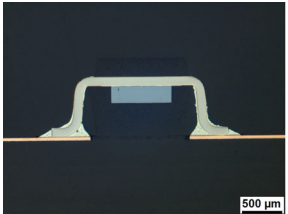
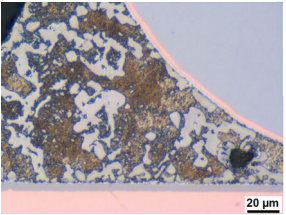
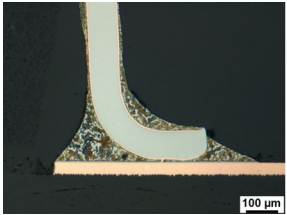
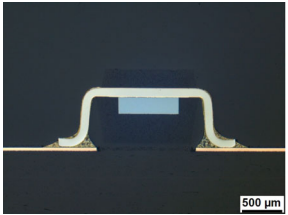
Fraunhofer ISIT

19

Cross section SOT363 after 1500 cycles TCT (-40°C/+85°C)

LTS

SAC



■ LTS and SAC, homogeneous intermetallic phase and intermetallic bond

■ LTS grain coarsening visible as an indication of TCT loading, but no cracks are visible

■ Discoloration of LTS solder due to etching

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.

© Fraunhofer ISIT 2022

X.

Fraunhofer ISIT

20

Helge Schimanski, Fraunhofer ISIT
LTS - Low temperature soldering

10

Cross section LFPAK56 after 1500 cycles TCT (-40°C/+85°C)

LTS

SAC

- LTS and SAC, homogeneous intermetallic phase and intermetallic bond
- LTS grain coarsening visible as an indication of TCT loading, but no cracks are visible

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022

21

Drop Test Result WLCSP12

LTS

SAC

- For LTS solder:
 - 9 PCBs with overall 108 devices were tested
 - The WLCSP12 samples passed the drop test requirement, > 100drops
 - 105 devices passed 3000 drops**
 - First failure occurred after 2824 drops
 - Fracture in RDL layer, see cross section
 - Indication of fracture in PCB pad
- For SAC solder:
 - 9 PCBs with overall 108 devices were tested
 - The WLCSP12 samples passed the drop test requirement, >100 drops
 - All 108 devices passed 3000 drops**

- LTS solder exceeding drop test requirement (>100 drops)**
- Failures as observed at >2800 drops may be related to the higher mechanical strength and hardness of LTS compared to SAC solder

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022

22

Summary of Results I: Processing / Assembly

- **Component wetting** according to ceramic plate test **is equally good** with SAC and LTS
- SPI shows **higher amount of solder paste** using LTS – this **depends on flux system**
- No significant difference between LTS and SAC in tilting performance
- X-Ray inspection show a few more voids in SAC, but uncritical
- Solder bridging occurs with DFN1010-6 using LTS (stencil apertures should be optimized)
- **No abnormalities in cross section:** Good wetting of both solder pastes, homogeneous intermetallic phases and bond
- **Good hybrid bond** for WLCSP12 between SAC balls and LTS solder due to diffusion in transition zone
- Shear strength is higher using LTS
- No difference in electrical performance measurable
- **All Nexperia packages can be soldered using SnBiX or SAC solder pastes**

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



23

Summary of Results II: Reliability

- Daisy chain of WLCSP12 & DFN1110D-3:
 - No failure in TCT -40°C/+85°C after 1500cycles with InSitu –monitoring
 - Drop test for LTS and SAC exceeds JEDEC requirements (> 100 drops)
- Devices in DSN0603, DF1010B-6, SOT363, LFPK56
 - No failure in TCT -40°C/+85°C after 1500cycles for LTS and SAC solder
 - No significant shift in electrical parameters after 1500cycles for LTS and SAC solder observed
- Shear test after TCT: Moderate reduction in shear force after TCT 1500cycles , acceptable for LTS and SAC
- Microsections after 1500 cycles -40°C/+85°C
 - Homogeneous intermetallic phases and intermetallic bond, no cracks observed using LTS solder
 - LTS grain coarsening visible as an indication of TCT loading, but no cracks are visible
- **All Nexperia packages show good reliability using SnBiX or SAC solder pastes**

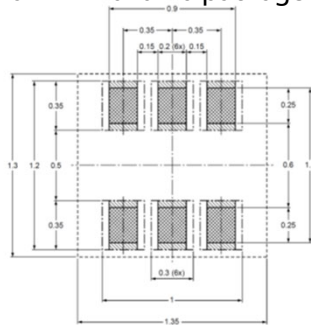
All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022







24

Stencil aperture recommendation for DFN1010-6 using LTS

Current footprint information for reflow soldering of DFN1010B-6 package



 solder land  solder land plus solder paste
 occupied area  solder resist
 Dimensions in mm

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.

© Fraunhofer ISIT 2022

Stencil aperture recommendation for DFN1010-6 using LTS

	Stencil aperture [μm x μm]	Radius [μm]	Area Ratio	Stencil thickness [μm]
Current	200 x 250	50	0,59	100
Possible	180 x 200	50	0,63	80
Possible	170 x 200	50	0,61	80
Preferred	160 x 200	50	0,59	80



Acknowledgments

A big thank to all who contributed to this investigation

- Hans-Jürgen Funke – Nexperia
- Jannik Entringer – Nexperia
- Andy Lippold – Nexperia
- Christian Liguda – Nexperia
- Jan Laehn – Fraunhofer ISIT
- Katja Reiter – Fraunhofer ISIT
- Alexander Barnbrock – Fraunhofer ISIT
- Kevin Byrd – Intel (technical advice of test execution)

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution, as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



Contact



Hans-Juergen Funke

Technical Director, Package Competence

Phone: +49 175 2954023

Hans-Juergen.Funke@nexperia.com

www.nexperia.com



Helge Schimanski

Fraunhofer Institute for Silicon Technology
Micro-Manufacturing Processes

Phone: +49 4821 17 4639

helge.schimanski@isit.fraunhofer.de

www.isit.fraunhofer.de

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution,
as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



27

Vielen Dank
für Ihre
Aufmerksamkeit!

H. Schimanski

All rights reserved, also regarding any disposal, exploitation, reproduction, editing, distribution,
as well as in the event of applications for property rights.
© Fraunhofer ISIT 2022



28